Exhibit A to the
Supplemental Declaration of Dr. Richard Blanchard
(declaration filed under seal)

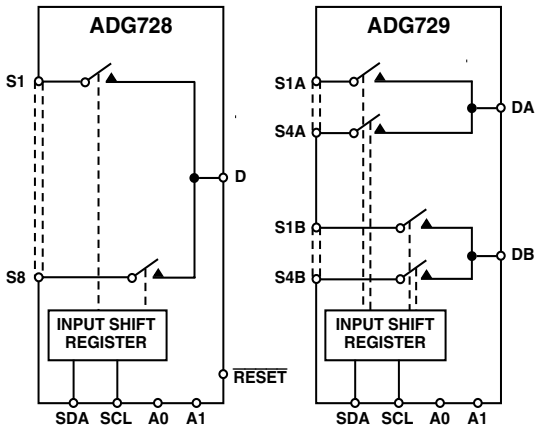
CMOS, Low-Voltage, 2-Wire Serially-Controlled, Matrix Switches

ADG728/ADG729

FEATURES
2-Wire Serial Interface
2.7 V to 5.5 V Single Supply
2.5 Ω On Resistance
0.75 Ω On-Resistance Flatness
100 pA Leakage Currents
Single 8-to-1 Matrix Switch ADG728
Dual 4-to-1 Matrix Switch ADG729
Power-On Reset
Small 16-Lead TSSOP Package

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching
Automatic Test Equipment

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG728 and ADG729 are CMOS analog matrix switches with a serially controlled 2-wire interface. The ADG728 is an 8-channel matrix switch, while the ADG729 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers, demultiplexers or switch arrays and the input signal range extends to the supplies.

The ADG728 and ADG729 utilize a 2-wire serial interface that is compatible with the I²C™ interface standard. Both have two external address pins (A0 and A1). This allows the 2 LSBs of the 7-bit slave address to be set by the user. Four of each of the devices can be connected to the one bus. The ADG728 also has a $\overline{\text{RESET}}$ pin that should be tied high if not in use.

Each channel is controlled by one bit of an 8-bit word. This means that these devices may be used in a number of different configurations; all, any, or none of the channels may be on at any one time.

On power-up of the device, all switches will be in the OFF condition and the internal shift register will contain all zeros.

All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

The ADG728 and ADG729 are available in 16-lead TSSOP packages.

PRODUCT HIGHLIGHTS

1. 2-Wire Serial Interface.
2. Single Supply Operation. The ADG728 and ADG729 are fully specified and guaranteed with 3 V and 5 V supply rails.
3. Low On Resistance 2.5 Ω typical.
4. Any configuration of switches may be on at any one time.
5. Guaranteed Break-Before-Make Switching Action.
6. Small 16-Lead TSSOP Package.

I²C is a trademark of Philips Corporation.

REV. A

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ADG728/ADG729–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4.5	5	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V, Test Circuit 2
	±0.1	±0.3	nA max	
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_D = 1 V/4.5 V, Test Circuit 3
	±0.1	±1	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 4.5 V/1 V, Test Circuit 4
	±0.1	±1	nA max	
LOGIC INPUTS (A0, A1)[2]				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	
		±0.1	μA max	
C_{IN}, Input Capacitance	6		pF typ	
LOGIC INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7 V_{DD}	V min	
		V_{DD} + 0.3	V max	
Input Low Voltage, V_{INL}		–0.3	V min	
		0.3 V_{DD}	V max	
I_{IN}, Input Leakage Current	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1.0	μA max	
V_{HYST}, Input Hysteresis	0.05 V_{DD}		V min	
C_{IN}, Input Capacitance	6		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	95		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		140	ns max	V_{S1} = 3 V
t_{OFF}	85		ns typ	V_{S1} = 3 V, R_L = 300 Ω, C_L = 35 pF;
		130	ns max	Test Circuit 5
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_{S1} = V_{S2} = 3 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG728	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG729	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG728	85		pF typ	
ADG729	42		pF typ	
C_D, C_S (ON)				
ADG728	96		pF typ	
ADG729	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		1.2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, Test Circuit 2
	±0.1	±0.3	nA max	
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 3 V/1 V, V_D = 1 V/3 V, Test Circuit 3
	±0.1	±1	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 3 V/1 V, Test Circuit 4
	±0.1	±1	nA max	
LOGIC INPUTS (A0, A1)[2]				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	
		±0.1	µA max	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7 V_{DD}	V min	
		V_{DD} + 0.3	V max	
Input Low Voltage, V_{INL}		–0.3	V min	
		0.3 V_{DD}	V max	
I_{IN}, Input Leakage Current	0.005		µA typ	V_{IN} = 0 V to V_{DD}
		±1.0	µA max	
V_{HYST}, Input Hysteresis	0.05 V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	130		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		200	ns max	V_{S1} = 2 V
t_{OFF}	115		ns typ	R_L = 300 Ω, C_L = 35 pF;
		180	ns max	V_S = 2 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_{S1} = V_{S8} = 2 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG728	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG729	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG728	85		pF typ	
ADG729	42		pF typ	
C_D, C_S (ON)				
ADG728	96		pF typ	
ADG729	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 3.3 V
		20	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 2.7 V to 5.5 V. All specifications –40°C to +85°C, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	ms min	SCL Cycle Time
t_2	0.6	ms min	t_{HIGH}, SCL High Time
t_3	1.3	ms min	t_{LOW}, SCL Low Time
t_4	0.6	ms min	$t_{HD, STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU, DAT}$, Data Setup Time
t_6[2]	0.9 0	ms max ms min	$t_{HD, DAT}$, Data Hold Time
t_7	0.6	ms min	$t_{SU, STA}$, Setup Time for Repeated Start
t_8	0.6	ms min	$t_{SU, STO}$, Stop Condition Setup Time
t_9	1.3	ms min	t_{BUF}, Bus Free Time Between a STOP Condition and a Start Condition
t_{10}	300 $20 + 0.1C_b$[3]	ns max ns min	t_R, Rise Time of Both SCL and SDA when Receiving
t_{11}	250 300 $0.1C_b$[3]	ns max ns max ns min	t_F, Fall Time of SDA when Receiving t_F, Fall Time of SDA when Transmitting
C_b	400	pF max	Capacitive Load for Each Bus Line
t_{SP}[4]	50	ns max	Pulsewidth of Spike Suppressed

NOTES
[1]See Figure 1.
[2]A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[3]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.
[4]Input filtering on both the SCL and SDA inputs suppress noise spikes which are less than 50 ns.

Specifications subject to change without notice.

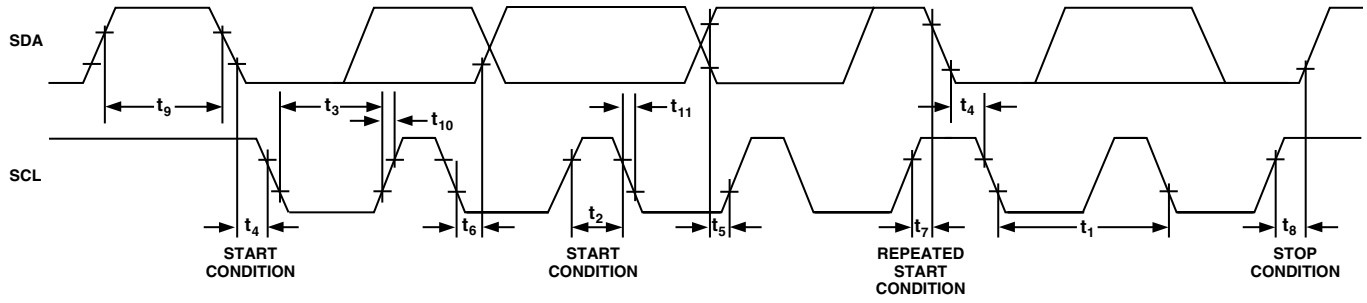


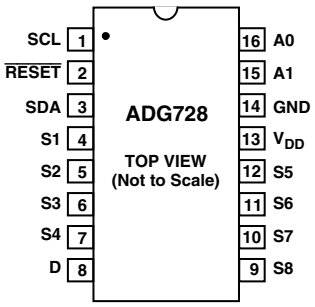
Figure 1. 2-Wire Serial Interface Timing Diagram

PIN FUNCTION DESCRIPTIONS

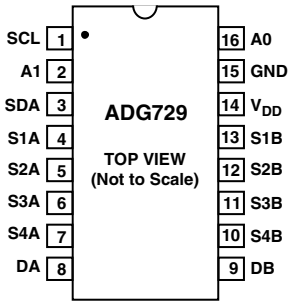
ADG728	ADG729	Mnemonic	Function
1	1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbit/s can be accommodated with this 2-wire serial interface.
2		$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back 1 byte of data during the read cycle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor.
4, 5, 6, 7	4, 5, 6, 7	Sxx	Source. May be an input or output.
8	8, 9	Dx	Drain. May be an input or output.
9, 10, 11, 12	10, 11, 12, 13	Sxx	Source. May be an input or output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	15	GND	Ground Reference.
15	2	A1	Address Input. Sets the second least significant bit of the 7-bit slave address.
16	16	A0	Address Input. Sets the least significant bit of the 7-bit slave address.

PIN CONFIGURATIONS

ADG728



ADG729



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG728BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG729BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted.)

V_{DD} to GND ..... –0.3 V to +7 V
Analog, Digital Inputs[2] ..... –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D ..... 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, Each S ..... 30 mA
Continuous Current D, ADG729 ..... 80 mA
Continuous Current D, ADG728 ..... 120 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C

TSSOP Package
θ_{JA} Thermal Impedance ..... 150.4°C/W
θ_{JC} Thermal Impedance ..... 27.6°C/W
Lead Temperature, Soldering (10 seconds) ..... 300°C
IR Reflow, Peak Temperature ..... 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG728/ADG729 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
I_{DD}	Positive Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match Between any Two Channels, i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF."
I_D (OFF)	Drain Leakage Current with the Switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON."
V_{INL}	Maximum Input Voltage for Logic "0."
V_{INH}	Minimum Input Voltage for Logic "1."
I_{INL} (I_{INH})	Input Current of the Digital Input.
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
t_{ON}	Delay time between the 50% and 90% points of the STOP condition and the switch "ON" condition.
t_{OFF}	Delay time between the 50% and 90% points of the STOP condition and the switch "OFF" condition.
t_D	"OFF" time measured between the 80% points of both switches when switching from one switch to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3 dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

Typical Performance Characteristics–ADG728/ADG729

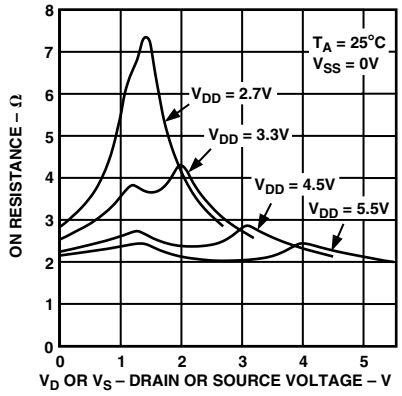


Figure 2. On Resistance as a Function of V_D (V_S) for Single Supply

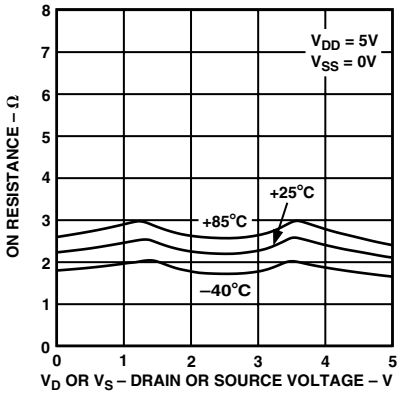


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

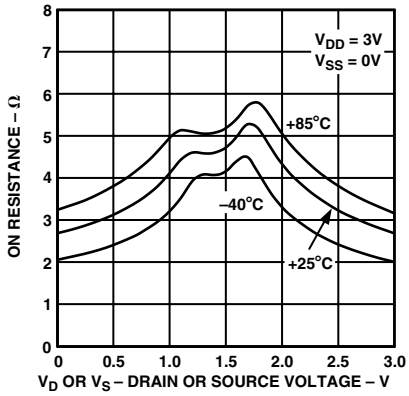


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

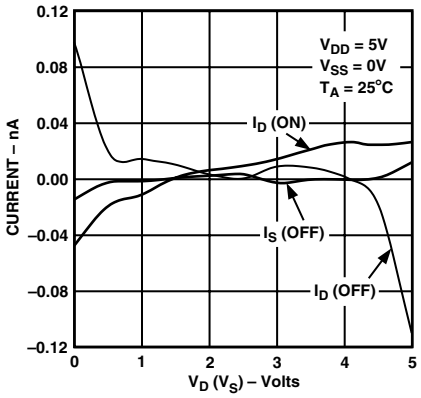


Figure 5. Leakage Currents as a Function of V_D (V_S)

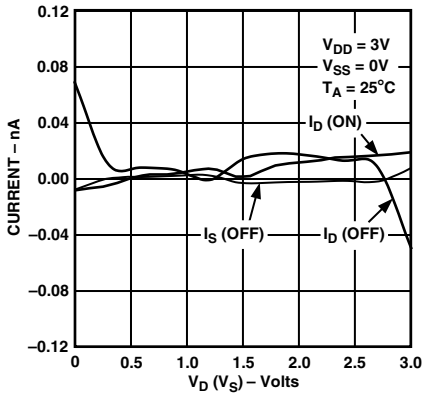


Figure 6. Leakage Currents as a Function of V_D (V_S)

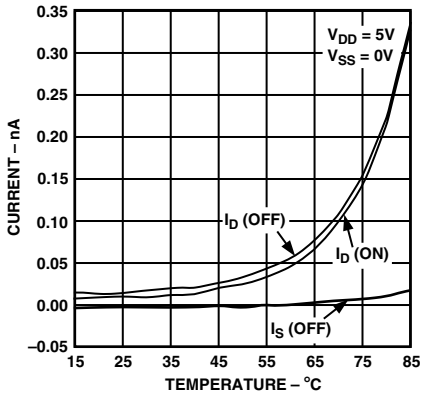


Figure 7. Leakage Currents as a Function of Temperature

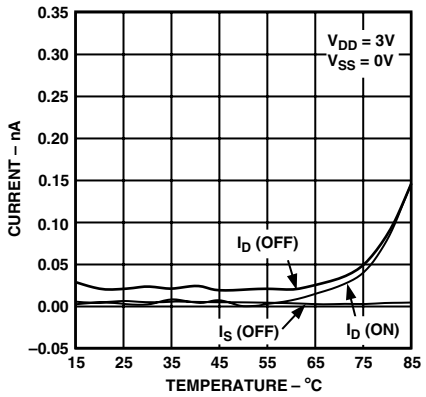


Figure 8. Leakage Currents as a Function of Temperature

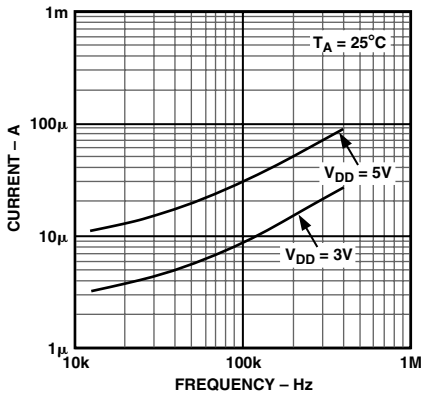


Figure 9. Input Current vs. Switching Frequency

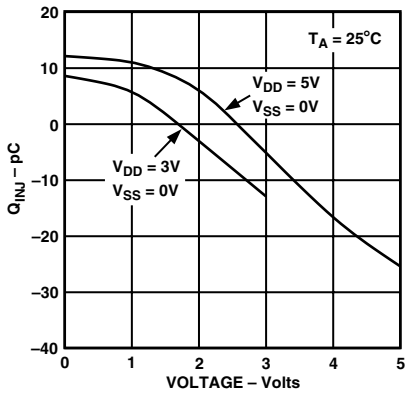


Figure 10. Charge Injection vs. Source Voltage

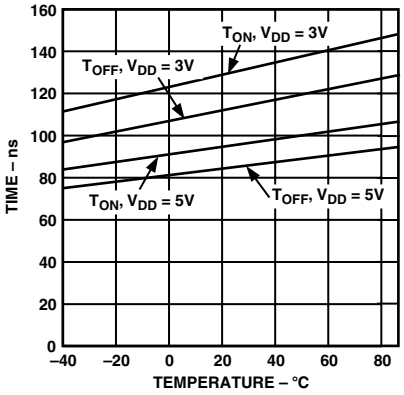


Figure 11. T_{ON}/T_{OFF} Times vs. Temperature

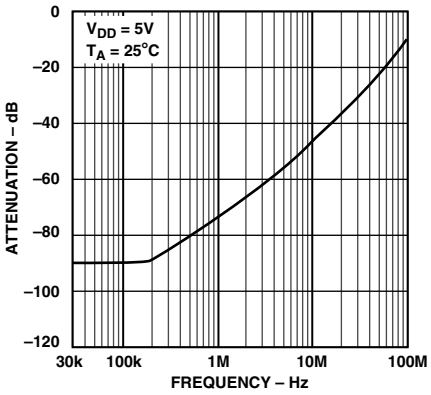


Figure 12. Off Isolation vs. Frequency

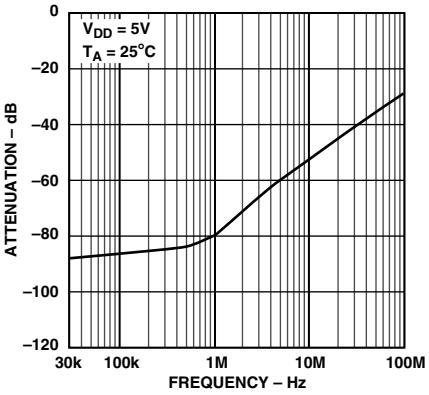


Figure 13. Crosstalk vs. Frequency

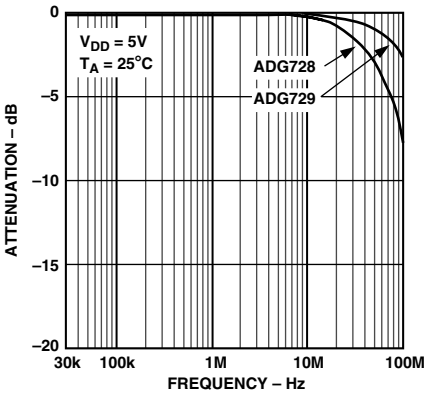


Figure 14. On Response vs. Frequency

GENERAL DESCRIPTION

The ADG728 and ADG729 are serially controlled, 8-channel and dual 4-channel matrix switches respectively. While providing the normal multiplexing and demultiplexing functions, these devices also provide the user with more flexibility as to where their signal may be routed. Each bit of the serial word corresponds to one switch of the device. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. In order to minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the ON condition, and is required to stay ON, there will be minimal glitches on the output of the switch.

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

2-Wire Serial Bus

The ADG728/ADG729 are controlled via an I^2C compatible serial bus. These parts are connected to this bus as a slave device (no clock is generated by the multiplexer).

The ADG728/ADG729 have different 7-bit slave addresses. The five MSBs of the ADG728 are 10011, while the MSBs of the ADG729 are 10001 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address followed by a R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master will read from the slave device. However, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse and then high during the tenth clock pulse to establish a STOP condition.

See Figures 18 to 21 below for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the matrix switch a number of times after addressing the part only once. During the write cycle, each data byte will update the configuration of the switches. For example, after the matrix switch has acknowledged its address byte, and receives one data byte, the switches will update after the data byte, if another data byte is written to the matrix switch while it is still the addressed slave device, this data byte will also cause an switch configuration update. Repeat read of the matrix switch is also allowed.

INPUT SHIFT REGISTER

The input shift register is eight bits wide. Figure 15 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1. The 8-bit word consists of eight data bits each controlling one switch. MSB (Bit 7) is loaded first.

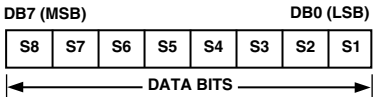


Figure 15. ADG728/ADG729 Input Shift Register Contents

WRITE OPERATION

When writing to the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operations for each matrix switch are shown in the figures below.

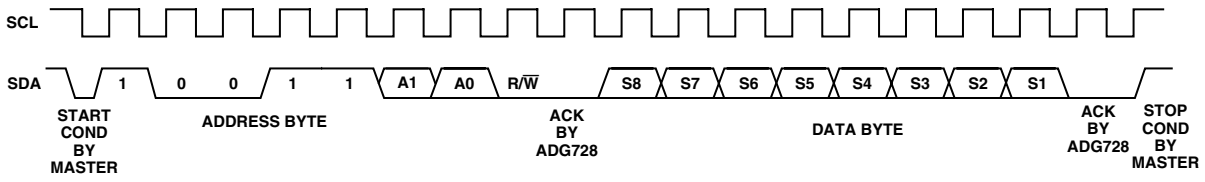


Figure 16. ADG728 Write Sequence

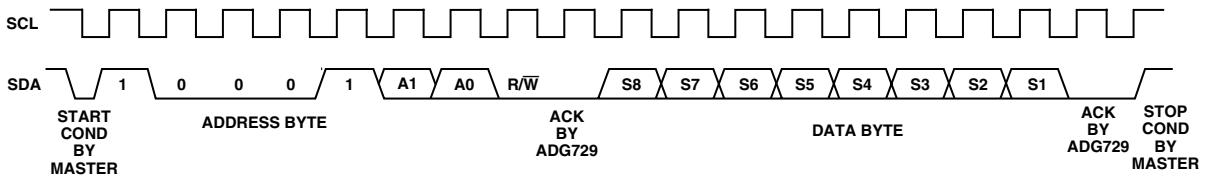


Figure 17. ADG729 Write Sequence

READ OPERATION

When reading data back from the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the matrix switch will acknowledge that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte that consists of the eight data bits in the input register. The read operations for each part are shown in Figures 18 and 19.

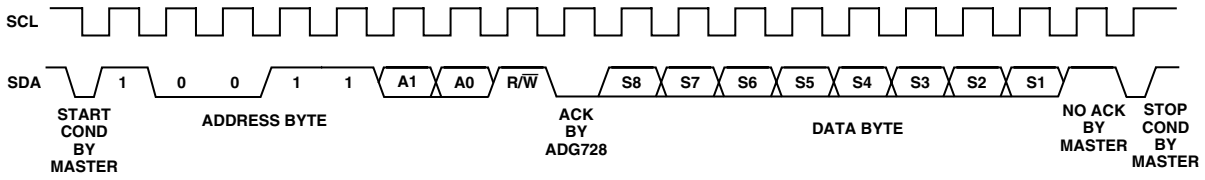


Figure 18. ADG728 Readback Sequence

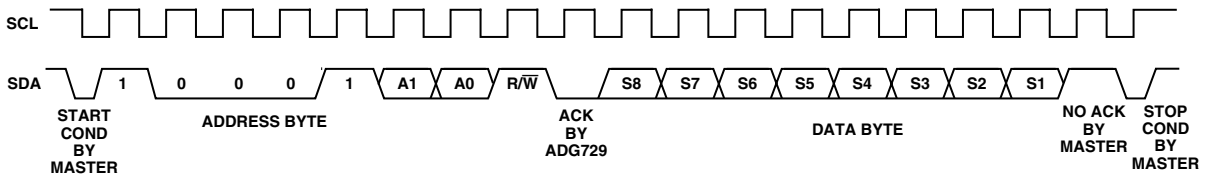


Figure 19. ADG729 Readback Sequence

MULTIPLE DEVICES ON ONE BUS

Figure 20 shows four ADG728s devices on the same serial bus. Each has a different slave address since the state of their A0 and A1 pins is different. This allows each Matrix Switch to be written to or read from independently. Because the ADG729 has a different address to the ADG728, it would be possible for four of each of these devices to be connected to the same bus.

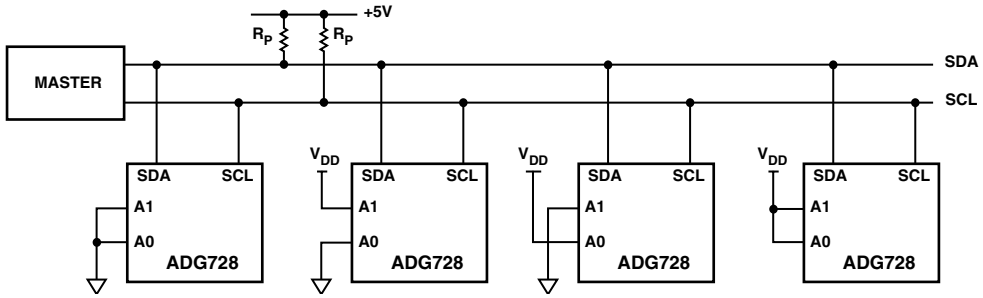
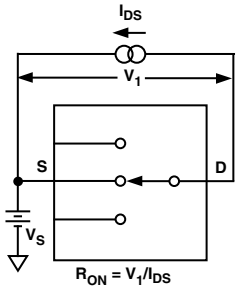
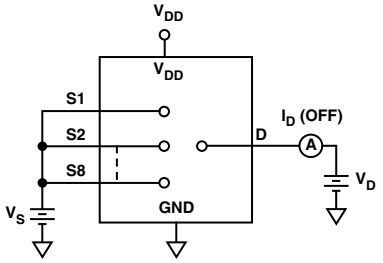


Figure 20. Multiple ADG728s on the Same Bus

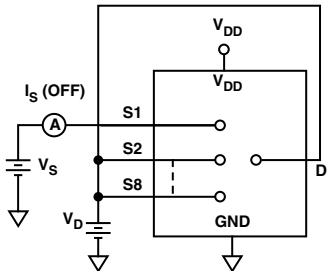
TEST CIRCUITS



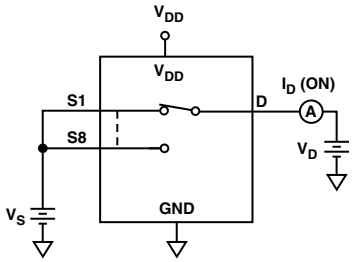
Test Circuit 1. On Resistance



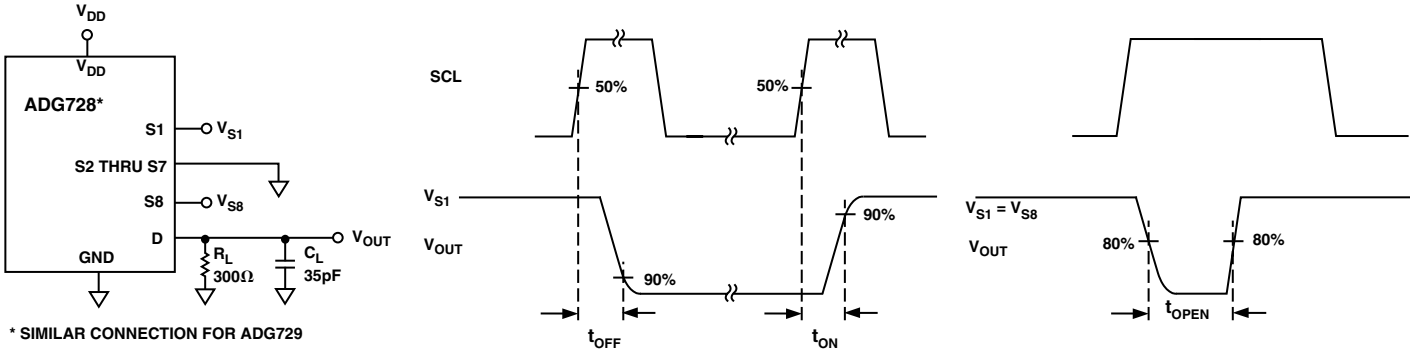
Test Circuit 3. I_S (OFF)



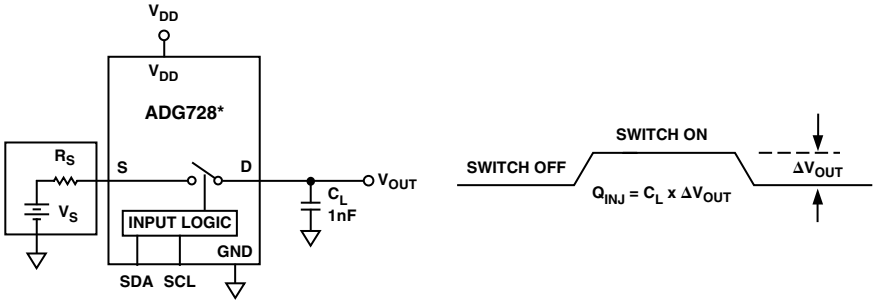
Test Circuit 2. I_D (OFF)



Test Circuit 4. I_D (ON)

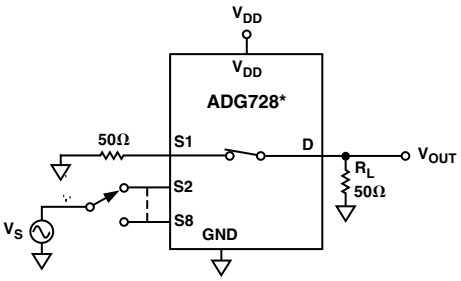


Test Circuit 5. Switching Times and Break-Before-Make Times



* SIMILAR CONNECTION FOR ADG729

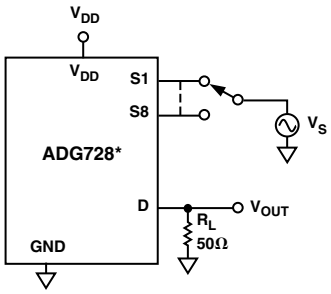
Test Circuit 6. Charge Injection



* SIMILAR CONNECTION FOR ADG729

CHANNEL-TO-CHANNEL CROSSTALK = $20LOG_{10}(V_{OUT}/V_S)$

Test Circuit 7. Channel-to-Channel Crosstalk



*SIMILAR CONNECTION FOR ADG729

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20LOG_{10}(V_{OUT}/V_S)$

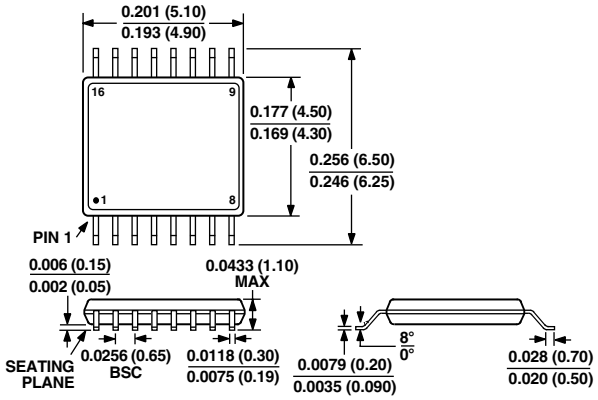
INSERTION LOSS = $20LOG_{10}\left(\frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}\right)$

Test Circuit 8. Off Isolation and Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)



19-1358; Rev 0; 4/98

MAXIM

Force-Sense Switches

General Description

The MAX4554/MAX4555/MAX4556 are CMOS analog ICs configured as force-sense switches for Kelvin sensing in automated test equipment (ATE). Each part contains high-current, low-resistance switches for forcing current, and higher resistance switches for sensing a voltage or switching guard signals. The MAX4554 contains two force switches, two sense switches, and two guard switches configured as two triple-pole/single-throw (3PST) normally open (NO) switches. The MAX4555 contains four independent single-pole/single-throw (SPST) normally closed (NC) switches, two force switches, and two sense switches. The MAX4556 contains three independent single-pole/double-throw (SPDT) switches, of which one is a force switch and two are sense switches.

These devices operate from a single supply of +9V to +40V or dual supplies of ±4.5V to ±20V. On-resistance (6Ω max) is matched between switches to 1Ω max. Each switch can handle Rail-to-Rail® analog signals. The off-leakage current is only 0.25nA at +25°C and 2.5nA at +85°C. The MAX4554 is also fully specified for +20V and -10V operation.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility.

Applications

Automated Test Equipment (ATE)

Calibrators

Precision Power Supplies

Automatic Calibration Circuits

Asymmetric Digital Subscriber Line (ADSL) with Loopback

Features

- **6Ω Force Signal Paths (±15V Supplies)**
  1Ω Force Signal Matching (±15V Supplies)
- **60Ω Sense-Guard Signal Paths (±15V Supplies)**
  8Ω Sense-Guard Signal Matching (±15V Supplies)
- **Rail-to-Rail Signal Handling**
- **Break-Before-Make Switching (MAX4556)**
- **t_{ON} and t_{OFF} = 275ns (±15V Supplies)**
- **Low 1µA Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4554CPE	0°C to +70°C	16 Plastic DIP
MAX4554CSE	0°C to +70°C	16 Narrow SO
MAX4554C/D	0°C to +70°C	Dice*
MAX4554EPE	-40°C to +85°C	16 Plastic DIP
MAX4554ESE	-40°C to +85°C	16 Narrow SO

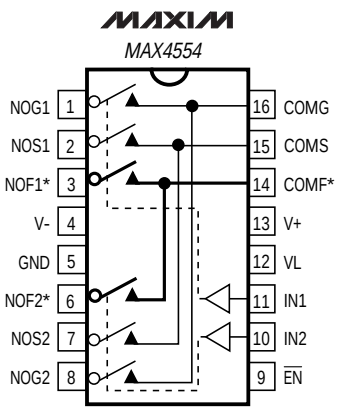
Ordering Information continued at end of data sheet.

**Contact factory for availability.*

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

MAX4554					
$\overline{EN}$	IN1	IN2	COMG	COMS	COMF*
1	X	X	OFF	OFF	OFF
0	0	0	OFF	OFF	OFF
0	0	1	NOG2	NOS2	NOF2*
0	1	0	NOG1	NOS1	NOF1*
0	1	1	NOG1 & NOG2	NOS1 & NOS2	NOF1* & NOF2*

NOTE: SWITCH POSITIONS SHOWN WITH IN_ = LOW
*INDICATES HIGH-CURRENT, LOW-RESISTANCE FORCE SWITCH
X = DON'T CARE

MAX4555/MAX4556 shown at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
V+ .....-0.3V to +44V
V- .....-25V to +0.3V
V+ to V-.....-0.3V to +44V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Force Terminals.....±100mA
Continuous Current into Any Other Terminal.....±30mA
Peak Current into Force Terminals
(pulsed at 1ms, 10% duty cycle).....±300mA
Peak Current into Any Other Terminal
(pulsed at 1ms, 10% duty cycle).....±100mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.7mW/°C above +70°C) 696mW
Operating Temperature Ranges
MAX455_C_ E .....0°C to +70°C
MAX455_E_ E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on analog or digital pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX4554 (+20V, -10V Supplies)

(V+ = +20V, V- = -10V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
6Ω ANALOG SWITCH (FORCE)							
Analog Signal Range	V_{COMF}, $V_{NOF\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	V_{COMF} = 10V, I_{COMF} = 10mA	+25°C		3.5	6	Ω
			C, E			7	
On-Resistance Match (Note 4)	ΔR_{ON}	V_{COMF} = 10V, I_{COMF} = 10mA	+25°C		0.4	1	Ω
			C, E			1.5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V_{COMF} = +5V, 0V, -5V; I_{COMF} = 10mA	+25°C		0.5	1.5	Ω
			C, E			2.0	
NOF_ Off-Leakage Current	$I_{NOF\_(OFF)}$	V+ = 22V, V- = -11V, V_{COMF} = ±10V, $V_{NOF\_}$ = ∓10V	+25°C	-0.25	0.03	0.25	nA
			C, E	-2.5		2.5	
COMF Off-Leakage Current	$I_{COMF(OFF)}$	V+ = 22V, V- = -11V, V_{COMF} = ±10V, $V_{NOF\_}$ = ∓10V	+25°C	-0.5	0.03	0.5	nA
			C, E	-2.5		2.5	
COMF On-Leakage Current	$I_{COMF(ON)}$	V+ = 22V, V- = -11V, V_{COMF} = ±10V	+25°C	-0.5	0.06	0.5	nA
			C, E	-10		10	
Charge Injection	Q	V_{COMF} = 0, Figure 13	C, E		80		pC
60Ω ANALOG SWITCH (SENSE-GUARD)							
Analog Signal Range	V_{COMS}, V_{COMG}, $V_{NOS\_}$, $V_{NOG\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	$V_{COM\_}$ = 10V, $I_{COM\_}$ = 1mA	+25°C		34	60	Ω
			C, E			70	
On-Resistance Match (Note 4)	ΔR_{ON}	$V_{COM\_}$ = 10V, $I_{COM\_}$ = 1mA	+25°C		5	8	Ω
			C, E			10	

ELECTRICAL CHARACTERISTICS—MAX4554 (+20V, -10V Supplies) (continued)

(V+ = +20V, V- = -10V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	$V_{COM\_}$ = +5V, 0V, -5V; $I_{COM\_}$ = 10mA	+25°C		3.5	9	Ω
			C, E			10	
NOS_, NOG_ Off-Leakage Current	$I_{NOS\_(OFF)}$, $I_{NOG\_(OFF)}$	V+ = 22V; V- = -11V; $V_{COM\_}$ = ±10V; $V_{NOS\_}$, $V_{NOG\_}$ = ±10V	+25°C	-0.25	0.02	0.25	nA
			C, E	-2.5		2.5	
COMS, COMG Off-Leakage Current	$I_{COMS(OFF)}$, $I_{COMG(OFF)}$	V+ = 22V; V- = -11V; $V_{COM\_}$ = ±10V; $V_{NOS\_}$, $V_{NOG\_}$ = ±10V	+25°C	-0.25	0.02	0.25	nA
			C, E	-2.5		2.5	
COMS, COMG On-Leakage Current	$I_{COMS(ON)}$, $I_{COMG(ON)}$	V+ = 22V, V- = -11V, $V_{COM\_}$ = ±10V	+25°C	-0.5	0.04	0.5	nA
			C, E	-5.0		5.0	
Charge Injection	Q	$V_{COM\_}$ = 0, Figure 13	+25°C		6		pC
LOGIC INPUT							
IN_, $\overline{EN}$ Input Logic Threshold High	V_{IN_H}, $V_{\overline{EN}H}$		C, E		1.6	2.4	V
IN_, $\overline{EN}$ Input Logic Threshold Low	V_{IN_L}, $V_{\overline{EN}L}$		C, E	0.8	1.6		V
IN_, $\overline{EN}$ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	$V_{IN\_}$ = $V_{\overline{EN}}$ = 0 or VL	C, E	-0.5	0.03	0.5	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Force)	t_{ON}	V_{COMF} = 3V, R_L = 300Ω, Figure 10	+25°C		150	300	ns
			C, E			350	
Turn-On Time (Sense-Guard)	t_{ON}	V_{COMS}, V_{COMG} = 10V; R_L = 1kΩ; Figure 10	+25°C		150	300	ns
			C, E			350	
Turn-Off Time (Force)	t_{OFF}	V_{COMF} = 3V, R_L = 300Ω, Figure 10	+25°C		130	300	ns
			C, E			350	
Turn-Off Time (Sense-Guard)	t_{OFF}	V_{COMS}, V_{COMG} = 10V; R_L = 1kΩ; Figure 10	+25°C		130	300	ns
			C, E			350	
Enable Time On	t_{EN}	$V_{COM\_}$ = 10V, Figure 11	+25°C		375	500	ns
			C, E			600	
Enable Time Off	t_{EN}	$V_{COM\_}$ = 10V, Figure 11	+25°C		170	275	ns
			C, E			350	
NOF_ Off-Capacitance	C_{OFF}	V_{NOF} = GND, f = 1MHz, Figure 14	+25°C		22		pF
NOS_, NOG_ Off-Capacitance	C_{OFF}	$V_{NOS\_}$, $V_{NOG\_}$ = GND; f = 1MHz; Figure 14	+25°C		7		pF
COMF Off-Capacitance	C_{OFF}	V_{COMF} = GND, f = 1MHz, Figure 14	+25°C		50		pF
COMS, COMG Off-Capacitance	C_{OFF}	V_{COMS}, V_{COMG} = GND; f = 1MHz; Figure 14	+25°C		15		pF
COMF On-Capacitance	C_{ON}	V_{COMF} = GND, f = 1MHz, Figure 14	+25°C		130		pF
COMS, COMG On-Capacitance	C_{ON}	V_{COMS}, V_{COMG} = GND; f = 1MHz; Figure 14	+25°C		30		pF
Total Harmonic Distortion (Force)	THD		+25°C		0.007		%
Off Isolation (Force)	V_{ISO}	$R_{IN\_}$ = 50Ω, R_{OUT} = 50Ω, f = 1MHz, $V_{COM\_}$ = 100mV_{RMS}, Figure 15	+25°C		-30		dB

ELECTRICAL CHARACTERISTICS—MAX4554 (+20V, -10V Supplies) (continued)

(V+ = +20V, V- = -10V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+, VL, V-	VL ≥ 4.5V	C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 22V; V- = -11V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or VL	+25°C	-1.0		1.0	µA
			C, E	-5.0		5.0	
V- Supply Current	I-	V+ = 22V; V- = -11V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or VL	+25°C	-1.0		1.0	µA
			C, E	-5.0		5.0	
VL Supply Current	I_{L+}	V+ = 22V; V- = -11V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or VL	+25°C	-1.0		1.0	µA
			C, E	-5.0		5.0	
Ground Current	I_{GND}	V+ = 22V; V- = -11V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or VL	+25°C	-1.0		1.0	µA
			C, E	-5.0		5.0	

ELECTRICAL CHARACTERISTICS—MAX4554 (±15V Supplies)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
6Ω ANALOG SWITCH (FORCE)							
Analog Signal Range	V_{COMF}, $V_{NOF\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	V_{COMF} = ±10V, I_{COMF} = 10mA	+25°C		4	6	Ω
			C, E			7	
On-Resistance Match (Note 4)	ΔR_{ON}	V_{COMF} = ±10V, I_{COMF} = 10mA	+25°C		0.5	1	Ω
			C, E			1.5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V_{COMF} = +5V, 0V, -5V; I_{COMF} = 10mA	+25°C		0.1	1	Ω
			C, E			1.5	
NOF_ Off-Leakage Current	$I_{NOF\_(OFF)}$	V+ = 16.5V, V- = -16.5V, V_{COMF} = ±10V, $V_{NOF\_}$ = ∓ 10V	+25°C	-0.25	0.03	0.25	nA
			C, E	-2.5		2.5	
COMF Off-Leakage Current	$I_{COMF(OFF)}$	V+ = 16.5V, V- = -16.5V, V_{COMF} = ±10V, $V_{NOF\_}$ = ∓ 10V	+25°C	-0.5	0.03	0.5	nA
			C, E	-5.0		5.0	
COMF On-Leakage Current	$I_{COMF(ON)}$	V+ = 16.5V, V- = -16.5V, V_{COMF} = ±10V	+25°C	-0.5	0.06	0.5	nA
			C, E	-10		10	
Charge Injection	Q	V_{COMF} = 0, Figure 13	+25°C		100		pC
60Ω ANALOG SWITCH (SENSE-GUARD)							
Analog Signal Range	V_{COMS}, V_{COMG}, $V_{NOS\_}$, $V_{NOG\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		38	60	Ω
			C, E			70	

ELECTRICAL CHARACTERISTICS—MAX4554 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
On-Resistance Match (Note 4)	ΔR_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		5	9	Ω
			C, E			10	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	$V_{COM\_}$ = +5V, 0V, -5V; $I_{COM\_}$ = 1mA	+25°C		1.5	5	Ω
			C, E			6	
NOS_, NOG Off-Leakage Current	$I_{NOS\_(OFF)}$, $I_{NOG\_(OFF)}$	V+ = 16.5V; V- = -16.5V; $V_{COM\_}$ = ±10V; $V_{NOS\_}$, $V_{NOG\_}$ = ∓10V	+25°C	-0.25	0.01	0.25	nA
			C, E	-2.5		2.5	
COMS, COMG Off-Leakage Current	$I_{COMS(OFF)}$, $I_{COMG(OFF)}$	V+ = 16.5V; V- = -16.5V; $V_{COM\_}$ = ±10V; $V_{NOS\_}$, $V_{NOG\_}$ = ∓ 10V	+25°C	-0.25	0.01	0.25	nA
			C, E	-2.5		2.5	
COMS, COMG On-Leakage Current	$I_{COMS(ON)}$, $I_{COMG(ON)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V	+25°C	-0.5	0.02	0.5	nA
			C, E	-5.0		5.0	
Charge Injection	Q	$V_{COM\_}$ = 0, Figure 13	+25°C		4		pC
LOGIC INPUT							
IN_, $\overline{EN}$ Input Logic Threshold High	V_{IN_H}, $V_{\overline{EN}H}$		C, E		1.6	2.4	V
IN_, $\overline{EN}$ Input Logic Threshold Low	V_{IN_L}, $V_{\overline{EN}L}$		C, E	0.8	1.6		V
IN_, $\overline{EN}$ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}, $I_{\overline{EN}H}$, $I_{\overline{EN}L}$	$V_{\overline{EN}}$ = 0 or VL	C, E	-0.5	0.03	0.5	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Force)	t_{ON}	$V_{COM\_}$ = ±10V, R_L = 300Ω, Figure 10	+25°C		135	275	ns
			C, E			325	
Turn-On Time (Sense-Guard)	t_{ON}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 10	+25°C		135	225	ns
			C, E			275	
Turn-Off Time (Force)	t_{OFF}	$V_{COM\_}$ = ±10V, R_L = 300Ω, Figure 10	+25°C		170	275	ns
			C, E			325	
Turn-Off Time (Sense-Guard)	t_{OFF}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 10	+25°C		135	225	ns
			C, E			275	
Enable Time On	t_{EN}	$V_{COM\_}$ = ±10V, R_L = 300Ω, Figure 11	+25°C		310	500	ns
			C, E			600	
Enable Time Off	t_{EN}	$V_{COM\_}$ = ±10V, R_L = 300Ω, Figure 11	+25°C		170	300	ns
			C, E			400	
NOF_ Off-Capacitance	C_{OFF}	V_{NOF} = GND, f = 1MHz, Figure 14	+25°C		22		pF
NOS_, NOG_ Off-Capacitance	C_{OFF}	$V_{NOS\_}$, $V_{NOG\_}$ = GND; f = 1MHz; Figure 14	+25°C		9		pF
COMF Off-Capacitance	C_{OFF}	V_{COMF} = GND, f = 1MHz, Figure 14	+25°C		29		pF
COMS, COMG Off-Capacitance	C_{OFF}	$V_{COMS\_}$, $V_{COMG\_}$ = GND; f = 1MHz; Figure 14	+25°C		9		pF

ELECTRICAL CHARACTERISTICS—MAX4554 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
COMF On-Capacitance	C_{ON}	V_{COMF} = GND, f = 1MHz, Figure 14	+25°C		107		pF
COMS, COMG On-Capacitance	C_{ON}	V_{COMS}, $V_{COMG\_}$ = GND; f = 1MHz; Figure 14	+25°C		29		pF
Total Harmonic Distortion (Force)	THD		+25°C		0.007		%
Off Isolation (Force)	V_{ISO}	$R_{IN\_}$ = 50Ω, R_{OUT} = 50Ω, f = 1MHz, $V_{COM\_}$ = 100mV_{RMS}, Figure 15	+25°C		-30		dB
POWER SUPPLY							
Power-Supply Range	V+, VL, V-	VL ≥ 4.5V	C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
V- Supply Current	I-	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
VL Supply Current	I_{L+}	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
Ground Current	I_{GND}	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0		1.0	µA
			C, E	-5.0		5.0	

ELECTRICAL CHARACTERISTICS—MAX4555 (±15V Supplies)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
6Ω ANALOG SWITCH (FORCE)							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		3.8	6	Ω
			C, E			7	
On-Resistance Match (Note 4)	ΔR_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		0.3	1	Ω
			C, E			1.5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	$V_{COM\_}$ = +5V, 0V, -5V; $I_{COM\_}$ = 10mA	+25°C		0.05	1	Ω
			C, E			1.5	
NC_ Off-Leakage Current	$I_{NC\_(OFF)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V, $V_{NO\_}$ = ∓10V	+25°C	-0.25	0.03	0.25	nA
			C, E	-2.5		2.5	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V, $V_{NO\_}$ = ∓10V	+25°C	-0.5	0.03	0.5	nA
			C, E	-5.0		5.0	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V	+25°C	-0.5	0.06	0.5	nA
			C, E	-10		10	
Charge Injection	Q	$V_{COM\_}$ = 0, Figure 13	+25°C		100		pC

ELECTRICAL CHARACTERISTICS—MAX4555 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
30Ω ANALOG SWITCH (SENSE-GUARD)							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		15	30	Ω
			C, E			45	
On-Resistance Match (Note 4)	ΔR_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		0.6	4	Ω
			C, E			5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	$V_{COM\_}$ = +5V, 0V, -5V; $I_{COM\_}$ = 10mA	+25°C		0.6	5	Ω
			C, E			6	
NC_ Off-Leakage Current	$I_{NC\_(OFF)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V, $V_{NO\_}$ = ∓10V	+25°C	-0.3	0.01	0.3	nA
			C, E	-2.5		2.5	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V, $V_{NO\_}$ = ∓10V	+25°C	-0.3	0.01	0.3	nA
			C, E	-2.5		2.5	
COM_ On-Leakage Current	$I_{NC\_(ON)}$	V+ = 16.5V, V- = -16.5V, $V_{NC\_}$ = ±10V	+25°C	-0.6	0.02	0.6	nA
			C, E	-5.0		5.0	
Charge Injection	Q	$V_{COM\_}$ = 0, Figure 13	+25°C		4		pC
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}	$V_{IN\_}$ = 0.8V or 2.4V	C, E	-0.5	0.03	0.5	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Force)	t_{ON}	$V_{COM\_}$ = ±3V, R_L = 300Ω, Figure 10	+25°C		155	275	ns
			C, E			325	
Turn-On Time (Sense-Guard)	t_{ON}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 10	+25°C		125	225	ns
			C, E			275	
Turn-Off Time (Force)	t_{OFF}	$V_{COM\_}$ = ±3V, R_L = 300Ω, Figure 10	+25°C		190	275	ns
			C, E			325	
Turn-Off Time (Sense-Guard)	t_{OFF}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 10	+25°C		125	225	ns
			C, E			275	
COM_ Off-Capacitance (Force)	C_{OFF}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		29		pF
COM_ On-Capacitance (Sense-Guard)	C_{ON}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		9		pF
COM_ On-Capacitance (Force)	C_{ON}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		107		pF
COM_ Off-Capacitance (Sense-Guard)	C_{OFF}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		29		pF

ELECTRICAL CHARACTERISTICS—MAX4555 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
NC_ Off-Capacitance (Force)	C_{OFF}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		22		pF
NC_ Off-Capacitance (Sense-Guard)	C_{OFF}	$V_{COM\_}$, $V_{NO\_}$ = GND; f = 1MHz; Figure 14	+25°C		9		pF
Total Harmonic Distortion (Force)	THD		+25°C		0.007		%
Off Isolation (Force) (Note 6)	V_{ISO}	R_{IN} = 50Ω, R_{OUT} = 50Ω, f = 1MHz, $V_{COM\_}$ = 100mV_{RMS}, Figure 15	+25°C		-38		dB
POWER SUPPLY							
Power-Supply Range	V+, VL, V-		C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
V- Supply Current	I-	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
VL Supply Current	I_{L+}	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
Ground Current	I_{GND}	V+ = 16.5V; V- = -16.5V; $V_{\overline{EN}}$, $V_{IN\_}$ = 0 or V+	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	

ELECTRICAL CHARACTERISTICS—MAX4556 (±15V Supplies)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
6Ω ANALOG SWITCH (FORCE)							
Analog Signal Range	V_{COM1}, V_{NO1}, V_{NC1}	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	V_{COM1} = ±10V, I_{COM1} = 10mA	+25°C		3.8	6	Ω
			C, E			7	
On-Resistance Match (Note 4)	ΔR_{ON}	V_{COM1} = ±10V, I_{COM1} = 10mA	+25°C		0.3	1	Ω
			C, E			1.5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V_{COM1} = +5V, 0V, -5V; I_{COM1} = 10mA	+25°C		0.05	1	Ω
			C, E			1.5	
NO1, NC1 Off-Leakage Current	$I_{NO1(OFF)}$, $I_{NC1(OFF)}$	V+ = 16.5V; V- = -16.5V; V_{COM1} = ±10V; V_{NO1}, V_{NC1} = ∓10V	+25°C	-0.25	0.03	0.25	nA
			C, E	-2.5		2.5	
COM1 Off-Leakage Current	$I_{COM1(OFF)}$	V+ = 16.5V, V- = -16.5V, V_{COM1} = ±10V, V_{NO1} = ∓10V	+25°C	-0.5	0.03	0.5	nA
			C, E	-5.0		5.0	
COM1 On-Leakage Current	$I_{COM1(ON)}$	V+ = 16.5V, V- = -16.5V, V_{COM1} = ±10V	+25°C	-0.5	0.06	0.5	nA
			C, E	-10		10	
Charge Injection	Q	V_{COM1} = 0, Figure 13	+25°C		100		pC

ELECTRICAL CHARACTERISTICS—MAX4556 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
60Ω ANALOG SWITCH (SENSE-GUARD)							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)	C, E	V-		V+	V
On-Resistance	R_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		36	60	Ω
			C, E			70	
On-Resistance Match (Note 4)	ΔR_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 10mA	+25°C		5	9	Ω
			C, E			10	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	$V_{COM\_}$ = +5V, 0V, -5V; $I_{COM\_}$ = 10mA	+25°C		0.6	5	Ω
			C, E			6	
NO_, NC Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 16.5V; V- = -16.5V; $V_{COM\_}$ = ±10V; $V_{NO\_}$, $V_{NC\_}$ = ∓ 10V	+25°C	-0.25	0.01	0.25	nA
			C, E	-2.5		2.5	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V+ = 16.5V; V- = -16.5V; $V_{COM\_}$ = ±10V; $V_{NO\_}$, $V_{NC\_}$ = ∓10V	+25°C	-0.25	0.01	0.25	nA
			C, E	-2.5		2.5	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V+ = 16.5V, V- = -16.5V, $V_{COM\_}$ = ±10V	+25°C	-0.5	0.02	0.5	nA
			C, E	-5.0		5.0	
Charge Injection	Q	$V_{COM\_}$ = 0, Figure 13	+25°C		5		pC
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.6	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.6		V
IN_ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}	$V_{IN\_}$ = 0 or VL	C, E	-0.5	0.03	0.5	µA
SWITCH DYNAMIC CHARACTERISTICS							
Transition Time (Force)	t_{TRANS}	$V_{COM\_}$ = ±10V, R_L = 300Ω, Figure 10	+25°C		150	250	ns
			C, E			300	
Transition Time (Sense-Guard)	t_{TRANS}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 10	+25°C		125	225	ns
			C, E			275	
Break-Before-Make Time	t_{BBM}	$V_{COM\_}$ = ±10V, R_L = 1kΩ, Figure 12	+25°C	1	15		ns
NO1, NC1 Off-Capacitance (Force)	C_{OFF}	V_{NO1}, V_{NC1} = GND; f = 1MHz; Figure 14	+25°C		21		pF
COM1 On-Capacitance (Force)	C_{ON}	V_{COM1} = GND, f = 1MHz, Figure 14	+25°C		137		pF
NO_, NC_ Off-Capacitance (Sense-Guard)	C_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = GND; f = 1MHz; Figure 14	+25°C		7		pF
COM_ On-Capacitance (Sense-Guard)	C_{ON}	$V_{COM\_}$ = GND, f = 1MHz, Figure 14	+25°C		30		pF
Total Harmonic Distortion (Force)	THD		+25°C		0.007		%
Off Isolation (Force)	V_{ISO}	R_{IN} = 50Ω, R_{OUT} = 50Ω, f = 1MHz, $V_{COM\_}$ = 100mV_{RMS}, Figure 15	+25°C		-30		dB

ELECTRICAL CHARACTERISTICS—MAX4556 (±15V Supplies) (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

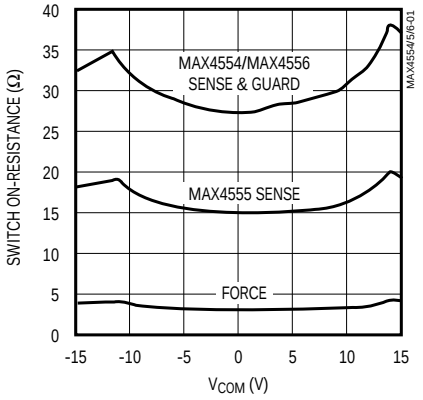
PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+, VL, V-	VL ≥ 4.5V	C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 16.5V, V- = -16.5V, $V_{IN\_}$ = 0 or VL	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
V- Supply Current	I-	V+ = 16.5V, V- = -16.5V, $V_{IN\_}$ = 0 or VL	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
VL Supply Current	I_{L+}	V+ = 16.5V, V- = -16.5V, $V_{IN\_}$ = 0 or VL	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5V, $V_{IN\_}$ = 0 or VL	+25°C	-1.0	0.001	1.0	µA
			C, E	-5.0		5.0	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal range.

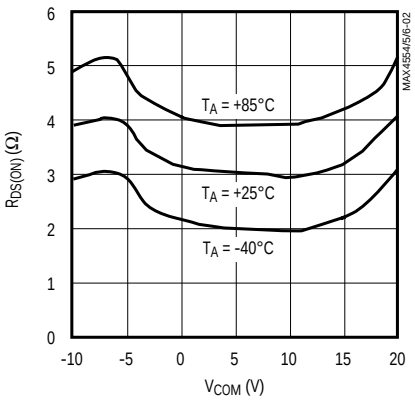
Typical Operating Characteristics

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

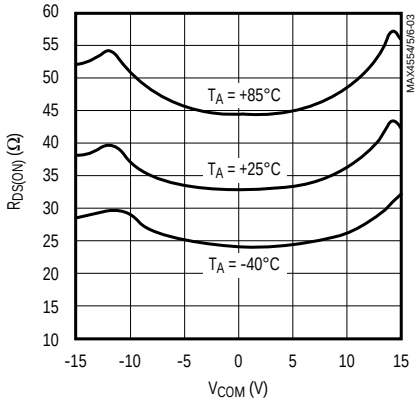
SWITCH ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



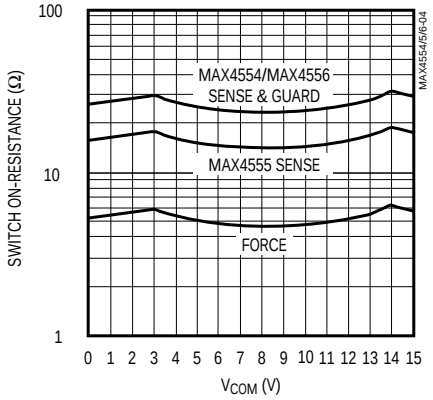
MAX4554 FORCE SWITCH ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



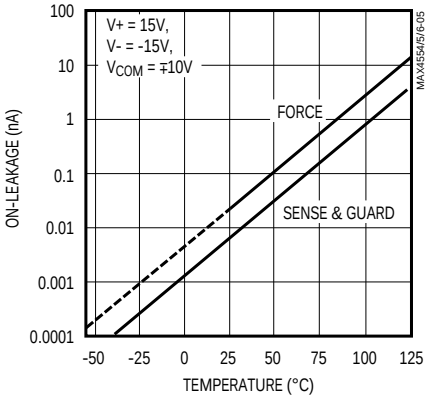
SENSE/GUARD SWITCH ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



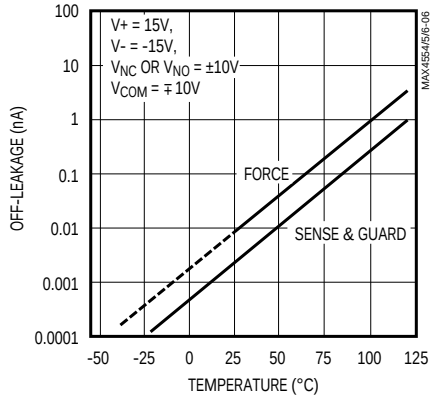
SWITCH ON-RESISTANCE vs. V_{COM} (SINGLE +15V SUPPLY)



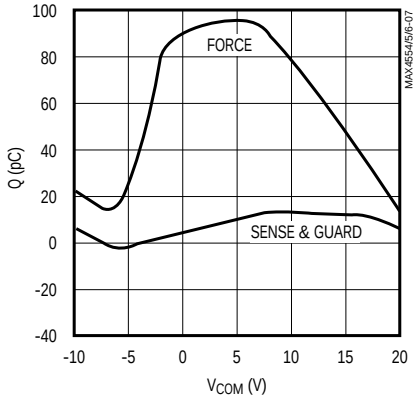
ON-LEAKAGE CURRENT vs. TEMPERATURE



OFF-LEAKAGE CURRENT vs. TEMPERATURE



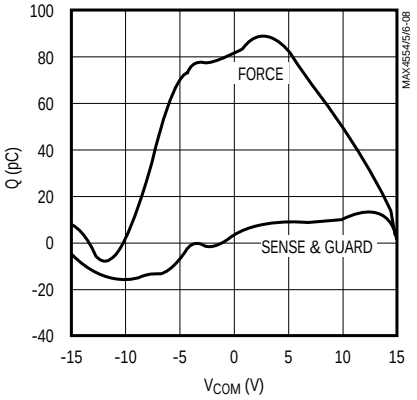
MAX4554 CHARGE INJECTION vs. V_{COM} (+20V, -10V SUPPLIES)



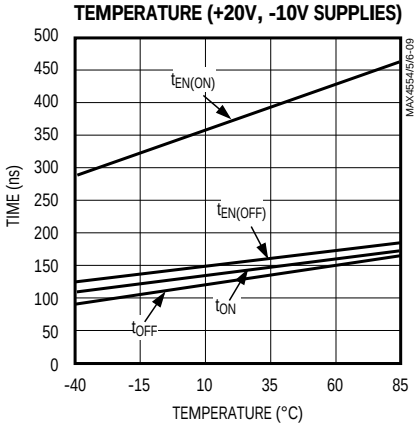
Typical Operating Characteristics (continued)

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

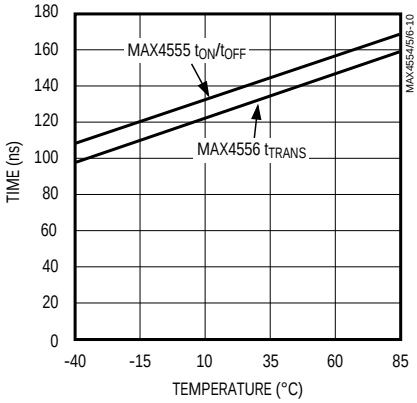
MAX4555/MAX4556
CHARGE INJECTION vs. V_{COM}
(+15V SUPPLIES)



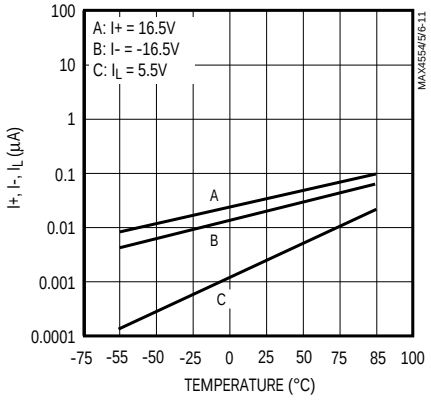
MAX4554
ON/OFF/ENABLE TIMES vs.
TEMPERATURE (+20V, -10V SUPPLIES)



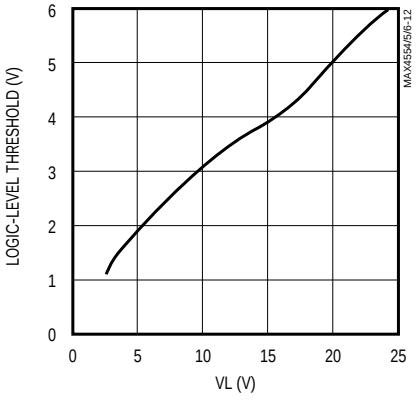
MAX4555/4556
ON/OFF/TRANSITION TIMES vs.
TEMPERATURE (+20V/-10V SUPPLIES)



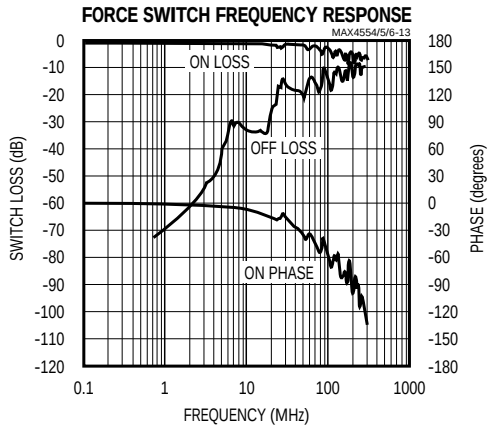
SUPPLY CURRENT
vs. TEMPERATURE



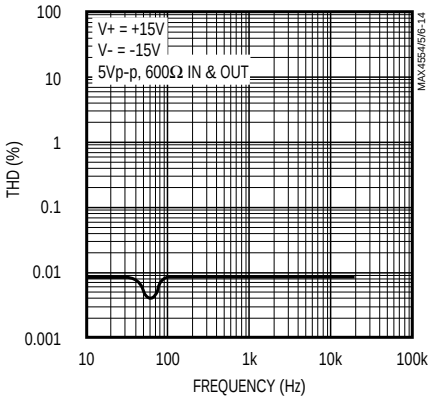
LOGIC-LEVEL THRESHOLD
vs. LOAD VOLTAGE



FORCE SWITCH FREQUENCY RESPONSE



FORCE SWITCH TOTAL HARMONIC
DISTORTION vs. FREQUENCY



Pin Description

PIN			NAME	FUNCTION
MAX4554	MAX4555	MAX4556		
1	—	—	NOG1	Analog Guard Channel 1 Normally Open Terminal
—	—	1, 2	NO3, NO2	Analog Signal Normally Open Terminals
2	—	—	NOS1	Analog Sense Channel 1 Normally Open Terminal
—	2, 15*, 10*, 7	14*, 15, 16	COM1, COM2 COM3, COM4	Analog Signal Common Terminals. COM2 and COM3 are low-resistance (force) switches on the MAX4555. COM1 is a low-resistance (force) switch on the MAX4556.
3*	—	—	NOF1*	Analog Force Channel 1 Normally Open Terminal
—	3, 14, 11, 6	—	NC1, NC2, NC3, NC4	Analog Signal Normally Closed Pins. NC2 and NC3 are low-resistance (force) switches.
—	—	3*	NO1*	Analog Force Signal Normally Open Terminal
4	4	4	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
5	5	5	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
6*	—	—	NOF2*	Analog Force Channel 2 Normally Open Terminal
—	—	6*	NC1*	Analog Force Signal Normally Closed Terminal
7	—	—	NOS2	Analog Sense Channel 2 Normally Open Terminal
—	—	7, 8	NC2, NC3	Analog Signal Normally Closed Terminal
8	—	—	NOG2	Analog Guard Channel 2 Normally Open Terminal
9	—	—	$\overline{EN}$	Enable Logic-Level Digital Input. Connect to GND to enable all switches.
11, 10	1, 16, 9, 8	9, 10, 11	IN1, IN2, IN3, IN4	Logic-Level Digital Inputs. See *Truth Tables.*
12	12	12	VL	Logic-Level Positive Supply Input. Connect to logic (+5V) supply. Can be connected to V+ for single-supply operation.
13	13	13	V+	Positive Analog Supply Voltage Input. Internally connected to substrate.
14*	—	—	COMF*	Analog Force Channel Common Terminal
15	—	—	COMS	Analog Sense Channel Common Terminal
16	—	—	COMG	Analog Guard Channel Common Terminal

** Indicates high-current, low-resistance (force) switch terminal.*

Note: *NO_, NC_, and COM_ pins are identical and interchangeable. Any may be considered as an input or output; signals pass equally well in either direction.*

Force-Sense Switches

Force-Sense Philosophy

When a precise voltage must be applied to a load that draws appreciable current, the resistance of the conductors connecting the source and the load can degrade the load voltage. The resistance of the conductors forms a voltage divider with the load, so that the load voltage is lower than the source voltage. The greater the distance between the source and the load, and the greater the current or conductor resistance, the greater the degradation. The resulting signal reduction can be overcome and the signal at the load guaranteed by using a 4-wire technique known as Kelvin sensing, or force-sense.

The basic idea behind the force-sense philosophy is to use four wires, forcing a voltage or current through two high-current wires to the load, and measuring (sensing) the voltage with two separate wires that carry very low or negligible current. One of two basic configurations is used, depending on whether or not feedback is employed:

1) The sensed voltage can be completely independent of the forced voltage or current, as in the case of a 4-wire ohmmeter, where a constant current is forced through one pair of wires and the voltage at the resistor is measured by another pair.
2) The sensed voltage can be part of a feedback circuit to force the load voltage to the desired value, as in the case of a 4-wire power supply. (In rare cases, this method is also used to measure resistance; the source is forced to produce a desired voltage in the resistor, and the source current required to achieve this voltage is measured.)

In all cases, the resistance of the high-current conductors can be ignored and the sensed voltage is an accurate measure of the load (or resistor's) voltage, despite appreciable voltage loss in the wires connecting the source and load.

There are two limitations to this scheme. First, the maximum source voltage (compliance) must be able to overcome the combined voltage loss of the load and the connecting wires. In other words, the conductors in the force circuit can have significant resistance, but there is a limit. Second, the impedance of the sensing circuit (typically a voltmeter, A/D converter, or feedback amplifier) must be very high compared to the load resistance and the sense wire resistance. These limitations are usually simple to overcome. The source compliance is usually required to be only a volt more than the load voltage, and the sense circuit usually has a multimegohm impedance. Typical 4-wire force-sense configurations are shown in Figure 1.

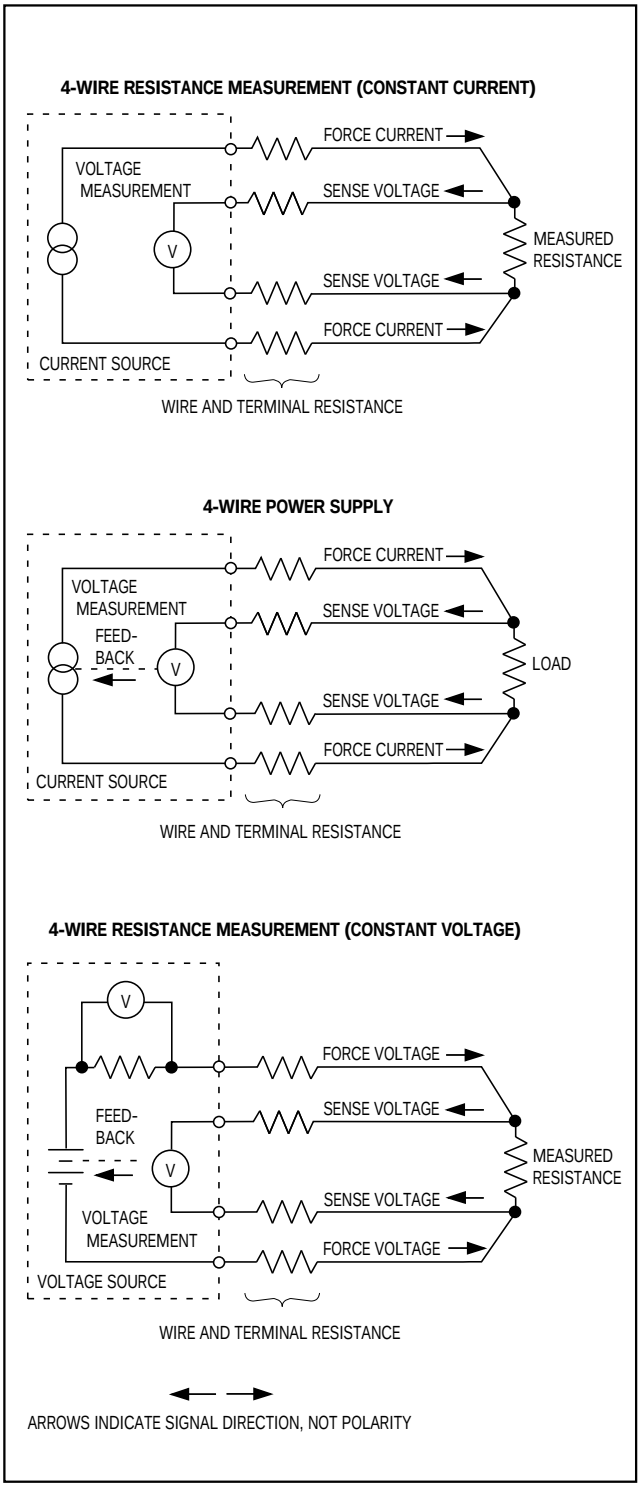


Figure 1. 4-Wire Force-Sense Measurements

Guard Philosophy

When measuring a precise voltage from a high-resistance source, or when measuring a very small current or forcing it into a load, unwanted leakage currents can degrade the results. These leakage currents may exist in the insulation of wires connecting the source and the measuring device. Higher source voltages, higher source impedances, longer wires, lower currents, and higher temperatures further degrade the measurement. The effect has both DC and low-frequency AC components; AC signals are generally capacitively coupled into the high-impedance source and wiring. The AC and DC effects are hard to separate, and are generally grouped under the designation “low-frequency noise.” This signal degradation can be overcome and the measured signal guaranteed by using a 3-wire technique known as guarding.

A “guard,” “guard channel,” or “driven guard” is formed by adding a third wire to a 2-wire measurement. It consists of a physical barrier (generally the surrounding shield of a coaxial cable) that is actively forced to the same voltage as is being measured on its inner conductor. The forcing of the driven guard is from the output of a low-impedance buffer amplifier whose high-impedance input is connected to the source. The idea is not just to buffer or shield the signal with a low-impedance source but, by forcing the shield to the same potential as the signal, to also force the leakage currents between the signal and the outside world to extremely small values. Any unwanted leakage current from the source must first go through the coaxial-cable insulation to the shield. Since the shield is at the same potential, there is virtually no unwanted leakage current, regardless of the insulation resistance. The shield itself can have significant leakage currents to the outside world, but it is separated from the measured signal.

The physical positioning of the guard around the signal is extremely important in maintaining low leakage. Since the guard can be at potentials far from ground, conventional coaxial cable is often replaced by triaxial cable (i.e., cable with a center conductor and two separate inner and outer shields). The signal is the center conductor, the inner shield is the guard, and the outer shield is the chassis ground. The outer shield isolates the inner driven guard from ground, physically protects the driven guard, and acts as a secondary Faraday shield for external noise.

The physical guard must be maintained continuously from the source to the measuring device, including paths on printed circuit boards, where the guard becomes extra traces surrounding the signal traces on both sides (and above and below the signal traces on multilevel boards.) This is one case where a ground plane is *not* appropriate. In extreme cases, such as with nano-voltmeters and femto-ammeters, printed circuit boards cannot be adequately shielded and are eliminated from the guarded signal paths altogether.

Figure 2 shows both the basic 3-wire guarded measurement and a 5-wire variation, used for balanced signals that are elevated from ground potential. The 5-wire configuration is really two 3-wire circuits sharing a common ground. Figure 2 also shows the configuration using triaxial cable.

Force-Sense-Guard Philosophy

Force-sense measurements are combined with guarded measurements when a wide range of voltages and currents are encountered, or when voltage and current must be accurately measured or controlled simultaneously. This frequently occurs in automatic test equipment (ATE) and in some critical physical or chemical sensor applications where voltage and/or current measurements can span many decades. Two techniques are used: 8-wire and 12-wire.

8-Wire Measurements

Figure 3 shows an 8-wire guarded force-sense power supply. A precise voltage is forced to the load, and load current is sensed without interacting with the output voltage, and without unwanted leakage currents. Separate twin-axial, or “twinax” cable is used for each of the positive and negative wires. Each cable has a twisted-pair of wires surrounded by a common shield, which is connected as the driven guard. Since the force and sense wires are at approximately the same potential, they can be protected by the same driven guard. In critical applications, two special 4-wire cables and connectors are substituted for the two twinax cables and separate ground wire. These cables add a second shield, which replaces the chassis-to-chassis ground wire and reduces noise.

Figure 3 shows current sensing with a fixed precision resistor and voltmeter, but other methods (such as op amps with feedback) are frequently employed, particularly if current limiting is required. One of the advantages of Figure 3’s circuit is that leakage in the current-sensing path has no effect on the output voltage.

The two diodes in the force-sense feedback path protect the force-sense amplifier from operating open loop if either the force or sense wires are disconnected from the load. These diodes must have both lower forward voltage and lower reverse leakage than the current being measured.

Force-Sense Switches

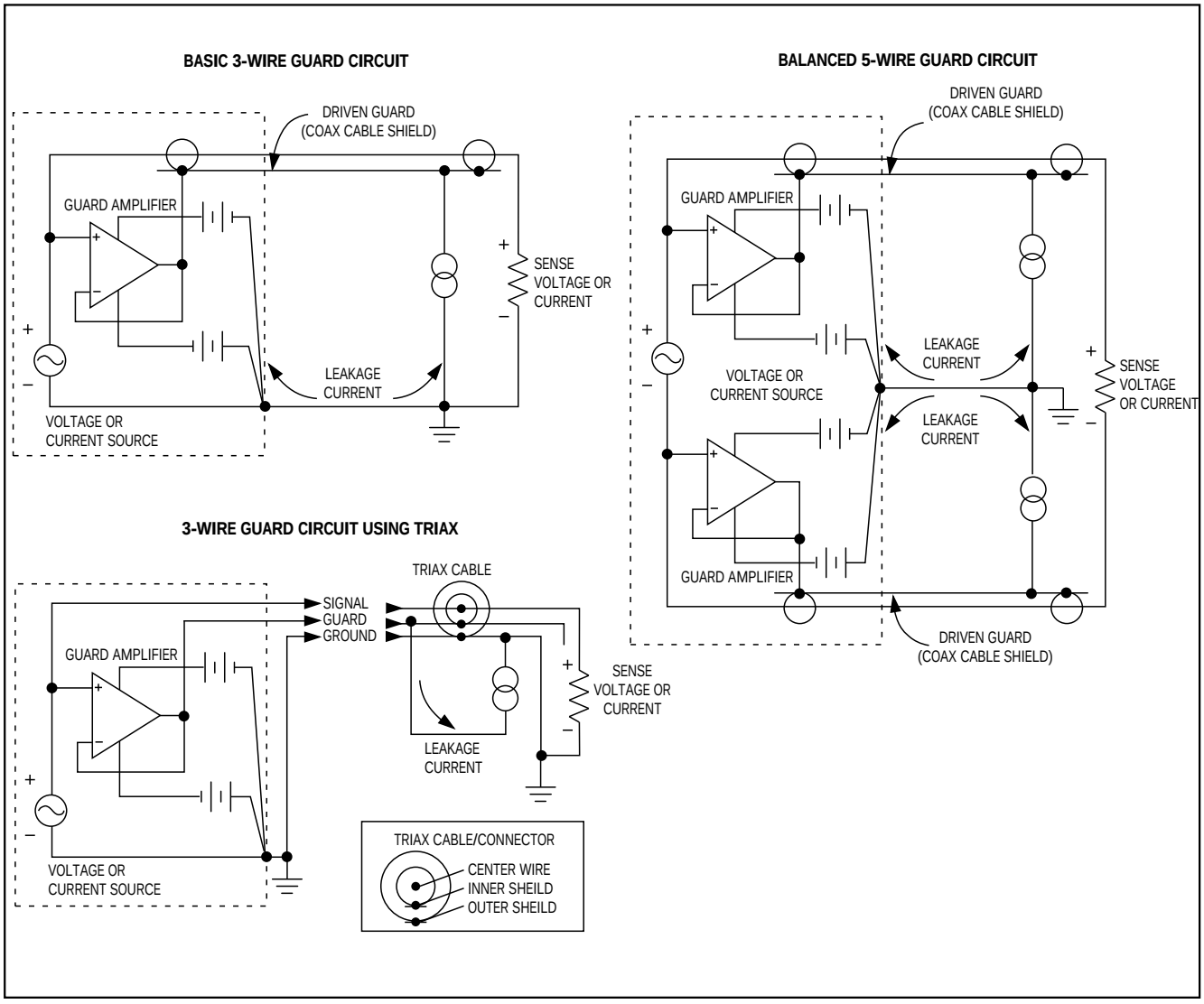


Figure 2. 3-Wire and 5-Wire Guarded Measurements

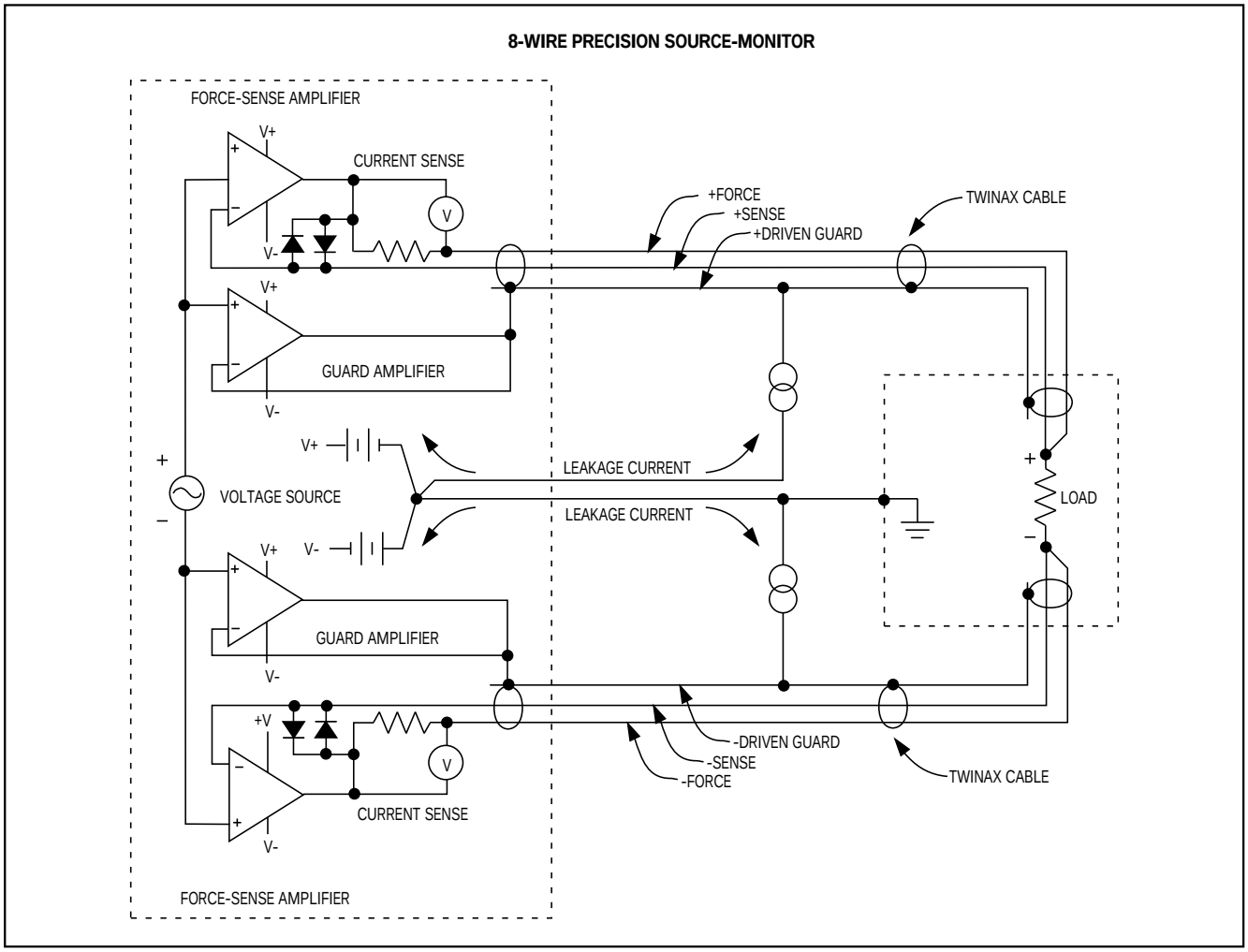


Figure 3. 8-Wire Guarded Force-Sense Measurements

Note that although the positive and negative circuits are identical, they are not redundant. Both are always used, even when one side of the load is grounded, because maintaining a precision output voltage requires losses in the ground leads to be corrected by a force-sense amplifier. If more than one power supply and load are operated together, and they have a common connection, this requirement becomes even more critical. Separate 8-wire connections prevent current changes in one load from changing voltage in the other load.

12-Wire Measurements

Figure 4 shows a 12-wire circuit, which is an elaboration of the 8-wire system using separate driven guards for the force and sense wires. Four sets of triaxial cables and connectors are used. The extra wires are used for two reasons: 1) They provide better shielding by having separate chassis grounds on each cable, rather than separate ground wires external to the signal cables; 2) In test equipment, where connection changes are frequent, it is very convenient to use four triax connectors or two quadrax (dual triax) connectors for each load.

In addition, this method is slightly better for power supplies or measurements that switch between constant voltage and constant current, since separate driven guards reduce circuit capacitance. Also, when troubleshooting, it is convenient to be able to interchange force and sense leads.

Force-Sense Switches

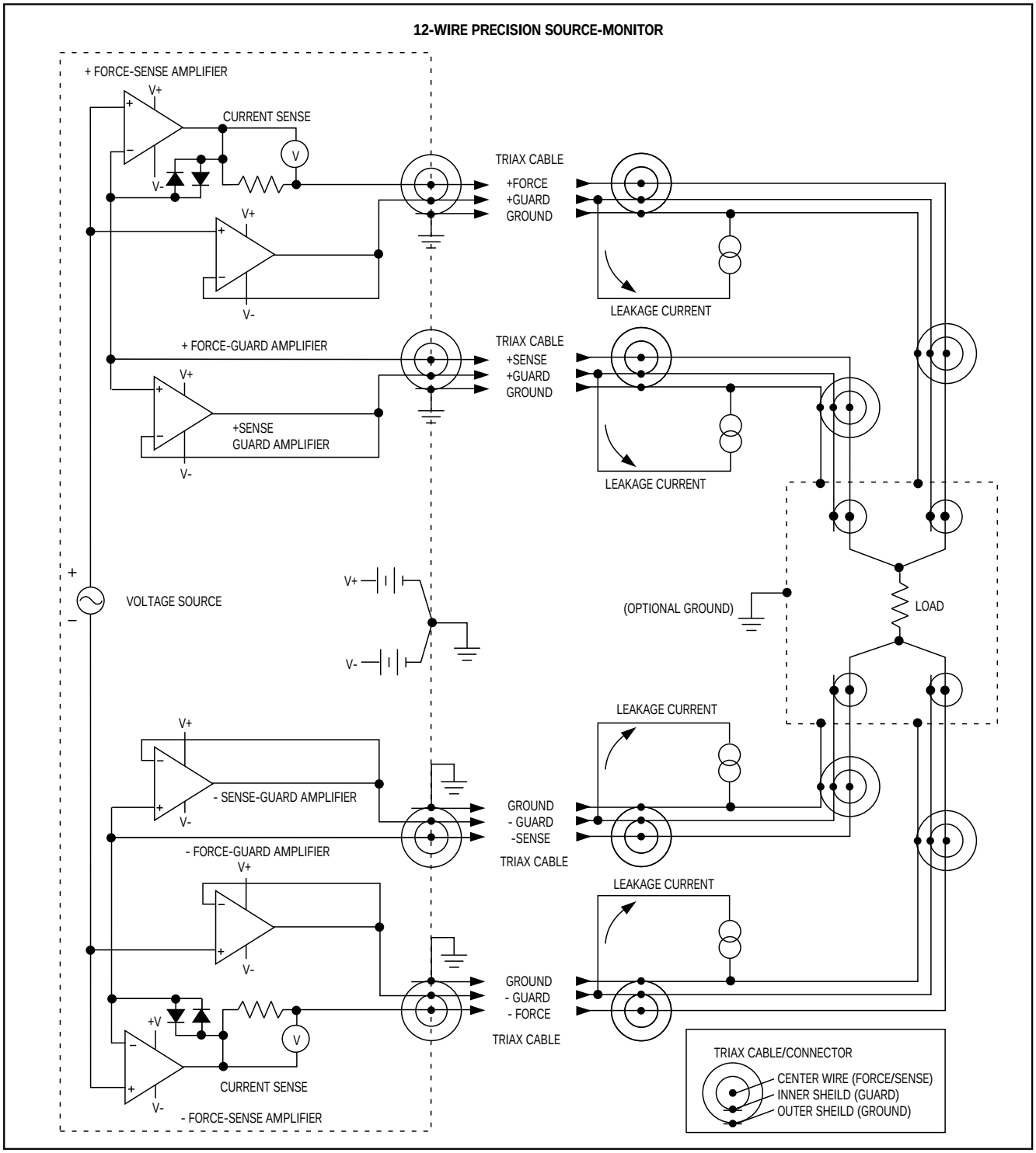


Figure 4. 12-Wire Guarded Force-Sense Measurements

Switching Guarded and Force-Sense Signals

When a precision source or measurement must be connected sequentially to several circuits, all sense and guard connections must be switched simultaneously, and at least one of the force connections must be switched. To maintain safety and low noise levels, the ground (or chassis) connection should never be disconnected.

The force circuit switch should have low-resistance, high-current capability, but the sense and guard circuit switches require only moderate resistance and current capability. The sense and guard switches should have lower leakage than the lowest measured current. CMOS switches should also be operated from power supplies higher than the highest circuit voltage to be switched.

Detailed Description

The MAX4554/MAX4555/MAX4556 are CMOS analog ICs configured as force-sense switches. Each part contains low-resistance switches for forcing current, and higher resistance switches for sensing a voltage or driving guard wires. Analog signals on the force, sense, or guard circuits can range from V- to V+. Each switch is completely symmetrical and signals are bidirectional; any switch terminal can be an input or output. The switches' open or closed states are controlled by TTL/CMOS-compatible input (IN_) pins.

The MAX4555 and MAX4556 are characterized and guaranteed only with ±15V supplies, but they can operate from a single supply up to +44V or non-symmetrical supplies with a voltage totaling less than +44V. The MAX4554 is fully characterized for operation from ±15V supplies, and it is also fully specified for operation with +20V and -10V supplies. A separate logic supply pin, VL, allows operation with +5V or +3V logic, even with unusual V+ values. The negative supply pin, V-, must be connected to GND for single-supply operation.

The MAX4554 contains two force switches, two sense switches, and two guard switches configured as two 3PST switches. The two switches operate independently of one another, but they have a common connection, allowing one source to be connected simultaneously to two loads, or two sources to be connected to one load. An enable pin, $\overline{EN}$, turns all switches off when driven to logic high. The MAX4554 is also fully specified for operation with +20V and -10V supplies. The MAX4555 contains four independent SPDT, NC switches; two are force switches and two are sense switches. The MAX4556 contains three independent SPDT switches; one is a force switch and two are sense switches.

Switch Resistances

Each IC contains four internal switches: four low-current sense-guard switches and two high-current force switches. Each sense-guard switch has an on-resistance of approximately 60Ω, while each force switch has an on-resistance of approximately 6Ω. The MAX4555's two low-current sense-guard switches are connected in parallel to produce lower on-resistance and allow higher current.

Power-Supply Considerations

Overview

The MAX4554/MAX4555/MAX4556's construction is typical of most CMOS analog switches. They have four supply pins: V+, V-, VL, and GND. V+ and V- are used to drive the internal CMOS switches and set the analog voltage limits on any switch. Reverse ESD protection diodes are internally connected between each analog and digital signal pin and both V+ and V-. If any signal exceeds V+ or V-, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from the signal paths.

Virtually all the analog leakage current comes through the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND or VL. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled, and their gates driven out of phase to V+ and V- by the logic-level translators.

VL and GND power the internal logic and logic-level translator and set the input logic threshold. The logic-level translator converts the logic levels to switched V+ and V- signals for driving the gates of the analog switches. This drive signal is the only connection between GND and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level inputs (IN_, and $\overline{EN}$) have ESD protection to V+ and V-, but not to GND; therefore, the logic signal can go below GND (as low as V-) when bipolar supplies are used. The logic-level threshold V_{IN} is CMOS and TTL compatible when VL is between 4.5V and 36V (see *Typical Operating Characteristics*).

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the internal P-channel switches, reducing the overall switch on-resistance. V- also sets the negative limit of the analog signal voltage.

Bipolar-Supply Operation

The MAX4554/MAX4555/MAX4556 operate with bipolar supplies between ±4.5V and ±18V. However, since all factory characterization is done with ±15V supplies (and +20V, -10V for MAX4554), operation at other supplies is not guaranteed. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 44V (see *Absolute Maximum Ratings*). VL must not exceed V+.

Single-Supply Operation

The MAX4554/MAX4555/MAX4556 operate from a single supply between +4.5V and +44V when V- is connected to GND. All of the bipolar precautions must be observed.

Applications Information

Switching 4-Wire Force-Sense Circuits

Figure 5 shows how to switch a single voltage or current source between two loads using two MAX4555s. A single CMOS inverter ensures that only one switch is on at a time. On each MAX4555, switches 2 and 3 are the high-current switches, so they should be used for force circuits. By interchanging loads and sources, the circuit can be reversed to switch two sources to a single load. Additional MAX4555s and loads or sources can be added to expand the circuit, but additional IN_ address decoding must be incorporated.

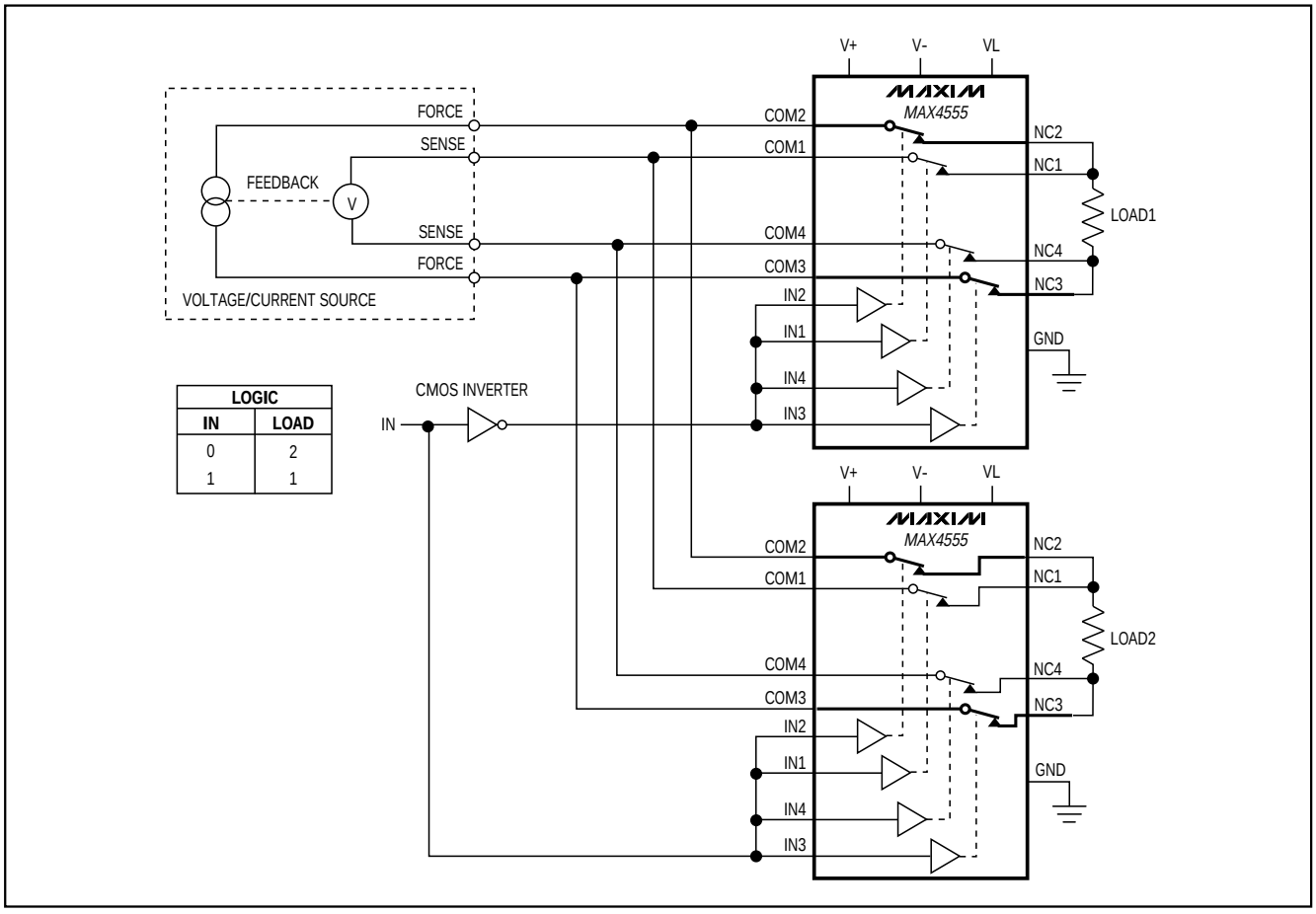


Figure 5. Using the MAX4555 to Switch 4-Wire Force-Sense Circuits from One Source to Two Loads

Figure 6 shows how to switch a single voltage or current source between two loads using the MAX4554 or MAX4556. By interchanging loads and sources, the circuits can be reversed so that they switch two sources to a single load. The two loads are electrically connected together at one point, but may be physically separated. This means that one force wire does not need to be switched, but the corresponding sense wires do.

The MAX4554 has independent 3PST, NO switches driven out of phase by an external CMOS inverter, so that one switch is on while the other is off. If both switches were turned on at the same time, both loads would be connected, and the resulting voltage at either load would be close to (but not exactly equal to) the desired value; this would not cause any damage to the device.

Switching 3-Wire Guarded Circuits

Figure 7 shows how to switch a single guarded voltage or current source between two loads using the MAX4554 or MAX4556. By interchanging loads and sources, the circuits can be reversed to switch two sources to a single load. If the loads have a common connection, the switch to that node can be eliminated.

Note that these circuits use sense (high-resistance) switches to switch the common wire. This is permissible only if the load currents are very low. If the currents are high, the common connection should not be switched unless another force switch is substituted.

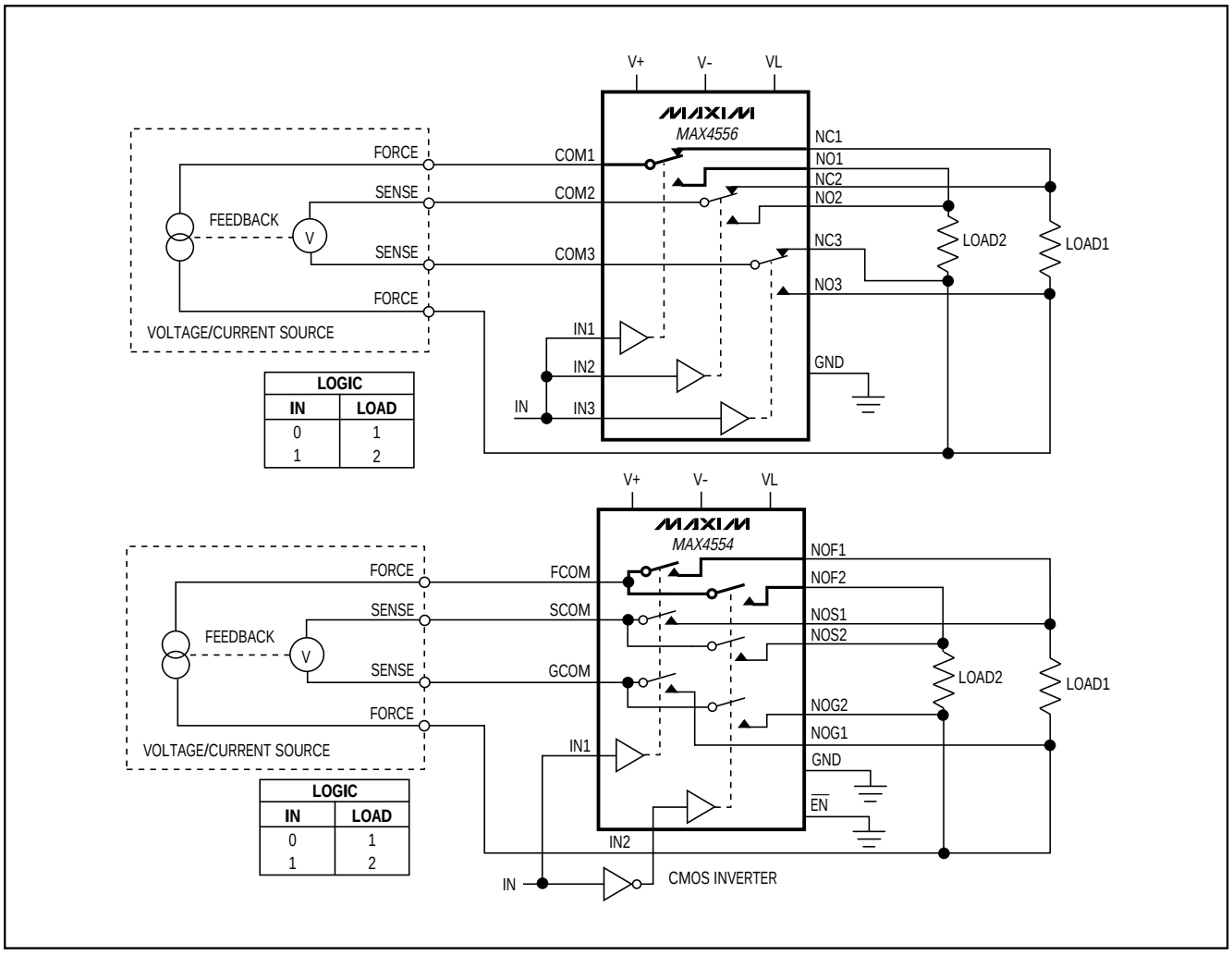


Figure 6. Using the MAX4554/MAX4556 to Switch 4-Wire Force-Sense Circuits from One Source to Two Loads

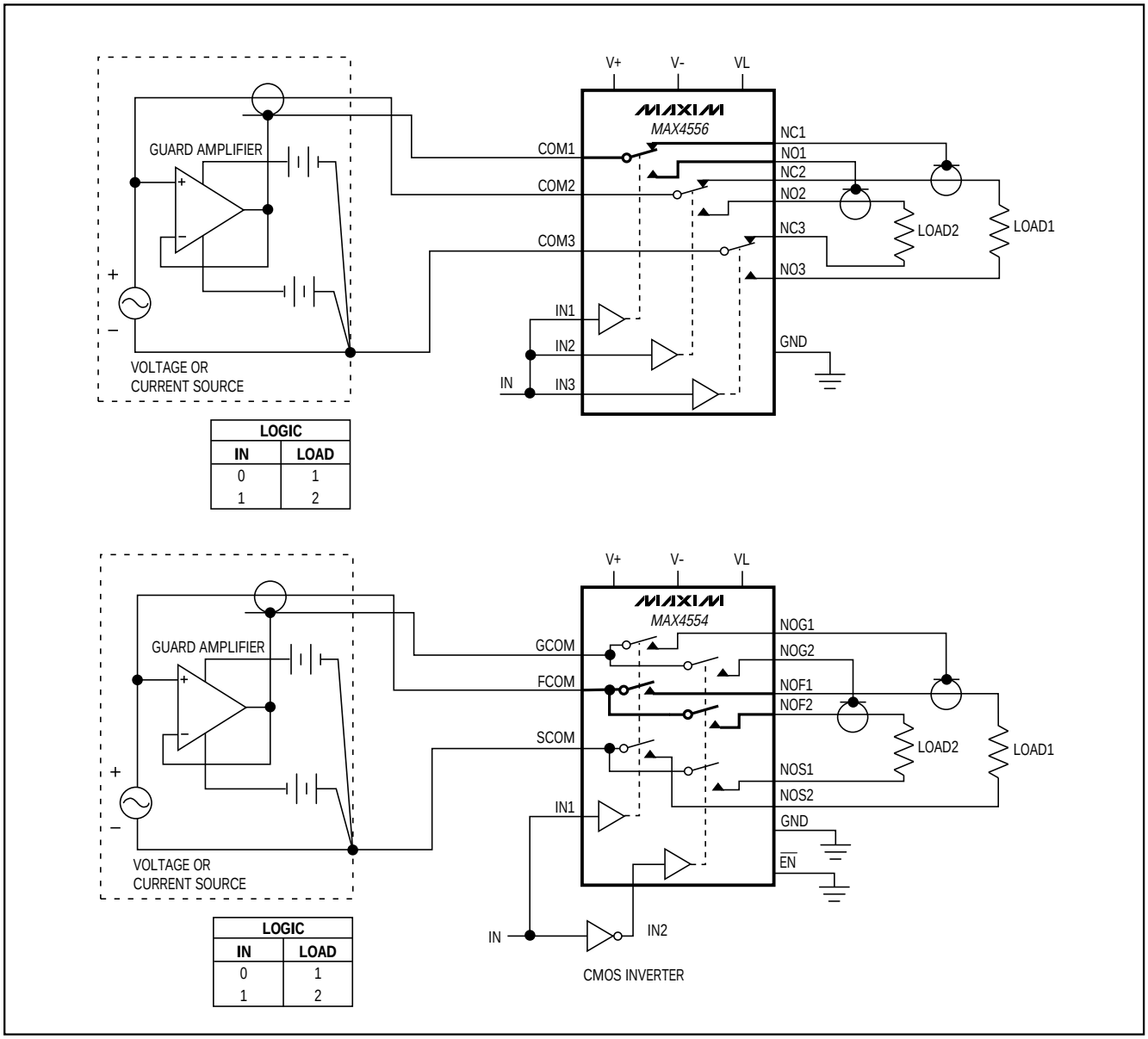


Figure 7. Using the MAX4554/MAX4556 to Switch 3-Wire Guarded Circuits from One Source to Two Loads

Figure 8 shows how to switch a single guarded voltage or current source between two grounded loads using a MAX4555. By interchanging loads and sources, the circuits can be reversed so that two sources are switched to a single load.

Switching 8-Wire Guarded Circuits

Figure 9 shows how to switch a single 8-wire guarded force-sense voltage or current source between two loads using two MAX4556s or two MAX4554s. By interchanging loads and sources, the circuits can be reversed so that they switch two sources to a single load. The two loads are shown isolated from each another, but if they have a common connection then the circuit must remain as shown in order to maintain accurate load voltage.

High-Frequency Performance

Although switching speed is restricted, once a switch is in a steady state it exhibits good RF performance. In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). The force switches have lower on-resistance, so their insertion loss in 50Ω systems is lower. Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not turning the switches on, but turning them off. The off-state switches act like capacitors and pass higher frequencies with less attenuation. At 10MHz, off-isolation between input or output signals is approximately -30dB in 50Ω systems, degrading (approximately 20dB per decade) as frequency increases. Higher circuit impedances also degrade off-isolation.

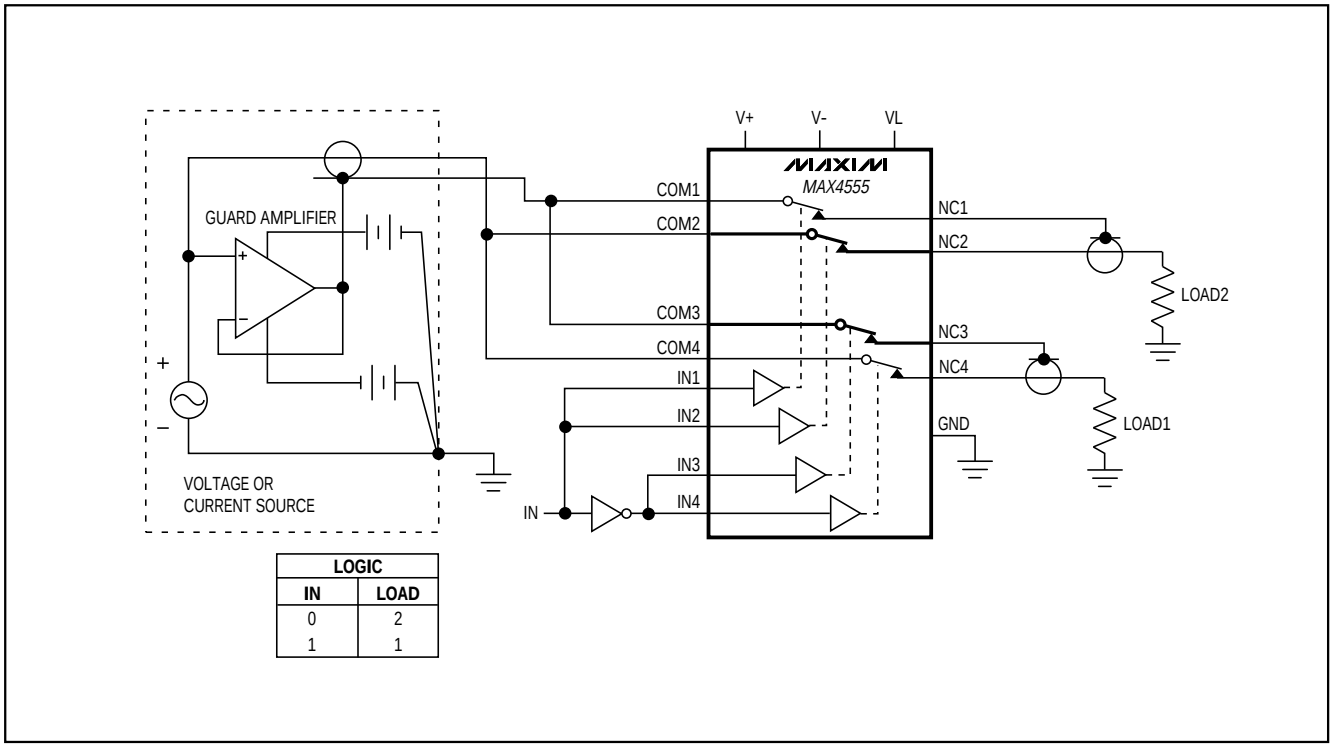


Figure 8. Using the MAX4555 to Switch 3-Wire Guarded Circuits from One Source to Two Loads

Force-Sense Switches

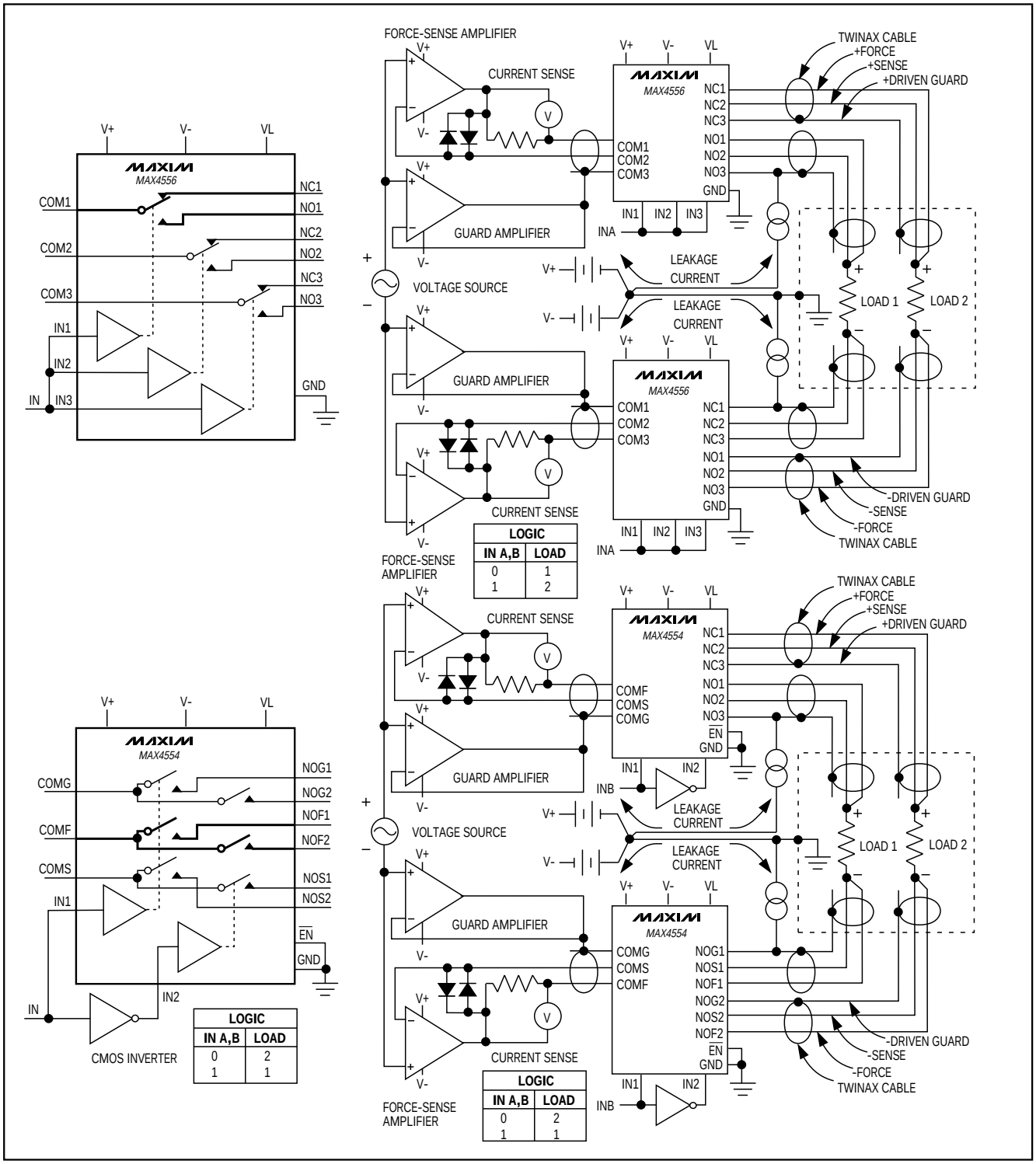


Figure 9. Switching 8-Wire Guarded Force-Sense Measurements from One Precision Source-Monitor to Two Loads

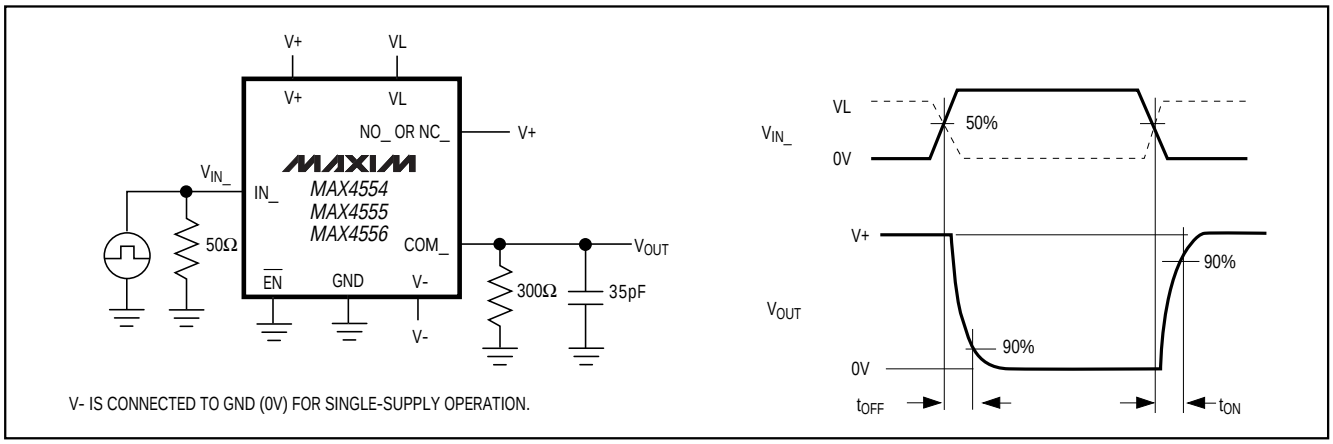


Figure 10. Address Transition Time

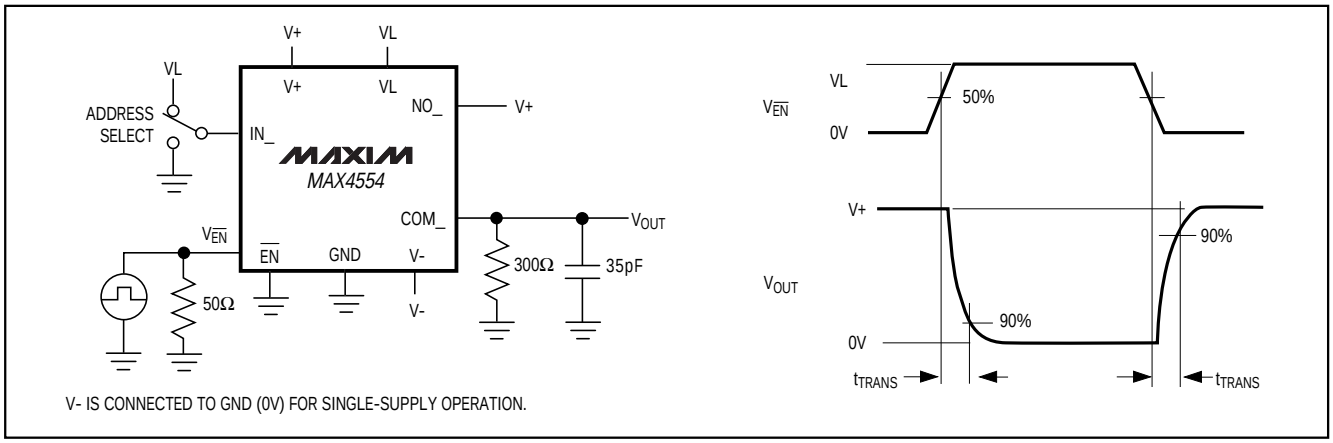


Figure 11. Enable Transition Time

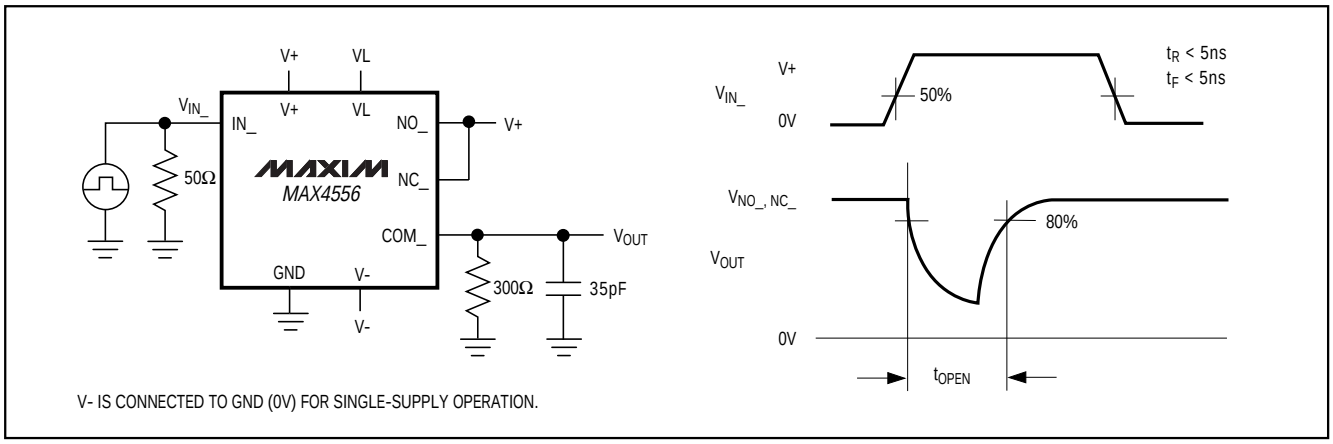


Figure 12. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

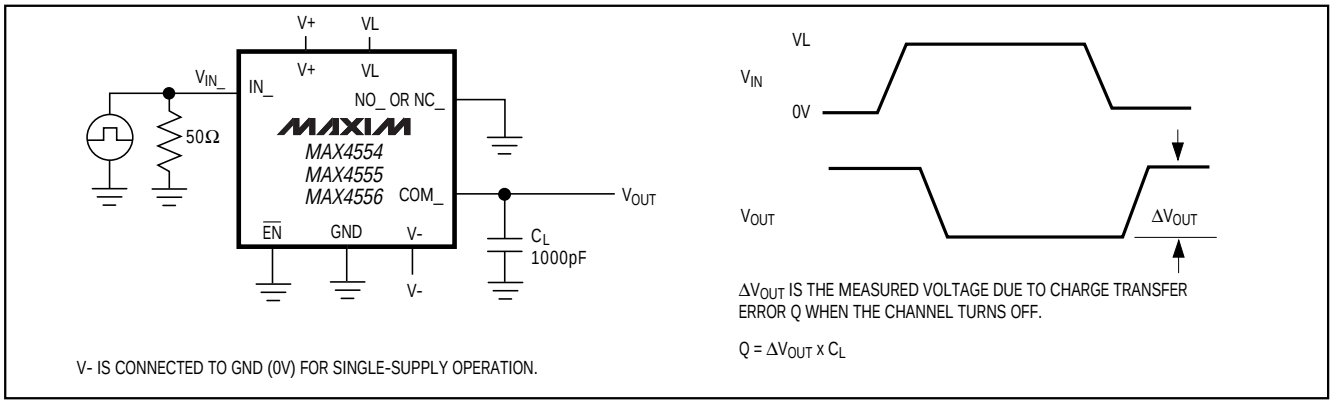


Figure 13. Charge Injection

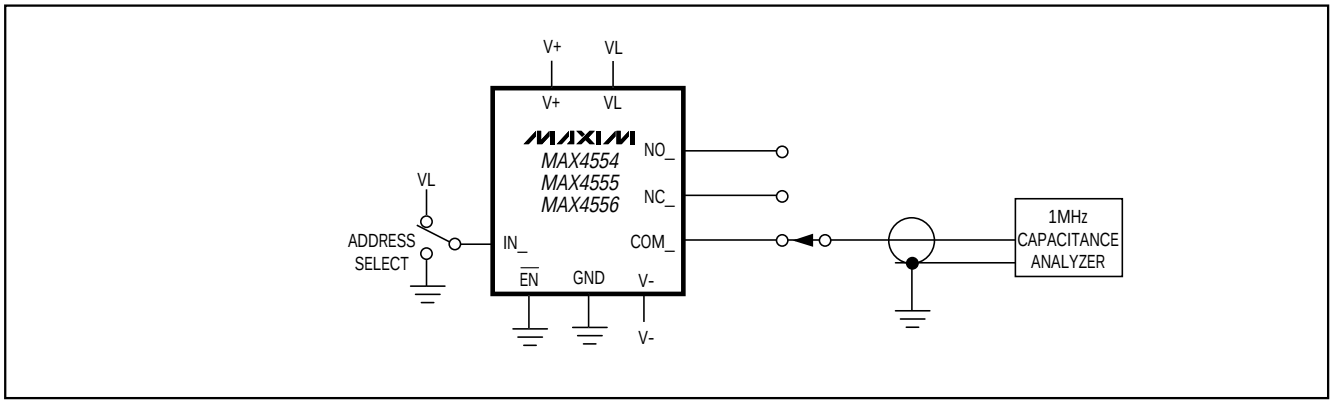


Figure 14. COM_, NO_, NC_ Capacitance

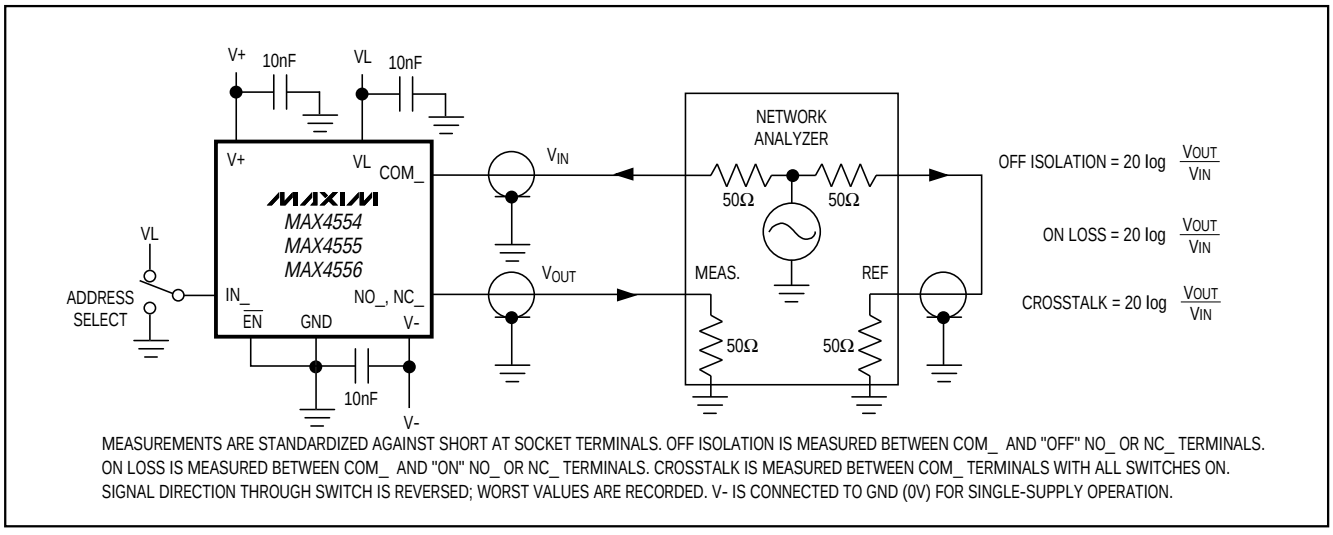
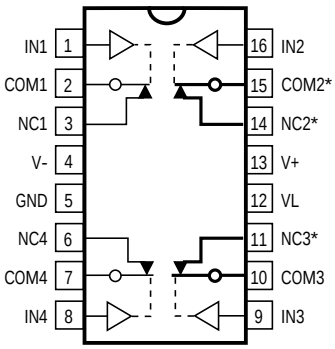


Figure 15. Frequency Response, Off-Isolation, and Crosstalk

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW

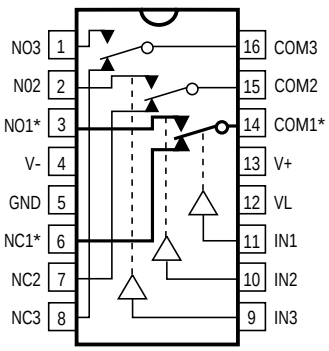
MAXIM
MAX4555



DIP/SO

MAX4555	
IN_	SWITCH
0	ON
1	OFF

MAXIM
MAX4556



DIP/SO

MAX4556	
IN_	COM_
0	NC_
1	NO_

SWITCH POSITIONS SHOWN WITH IN_ = LOW
*INDICATES HIGH-CURRENT, LOW-RESISTANCE FORCE SWITCH

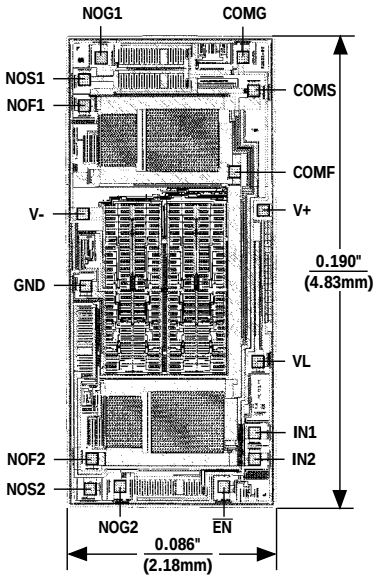
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4555CPE	0°C to +70°C	16 Plastic DIP
MAX4555CSE	0°C to +70°C	16 Narrow SO
MAX4555C/D	0°C to +70°C	Dice*
MAX4555EPE	-40°C to +85°C	16 Plastic DIP
MAX4555ESE	-40°C to +85°C	16 Narrow SO
MAX4556CPE	0°C to +70°C	16 Plastic DIP
MAX4556CSE	0°C to +70°C	16 Narrow SO
MAX4556C/D	0°C to +70°C	Dice*
MAX4556EPE	-40°C to +85°C	16 Plastic DIP
MAX4556ESE	-40°C to +85°C	16 Narrow SO

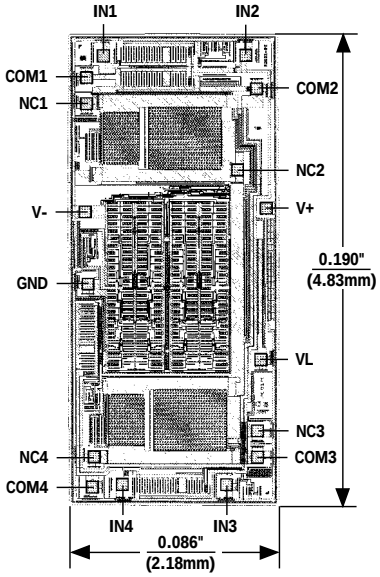
Contact factory for availability.

Chip Topographies

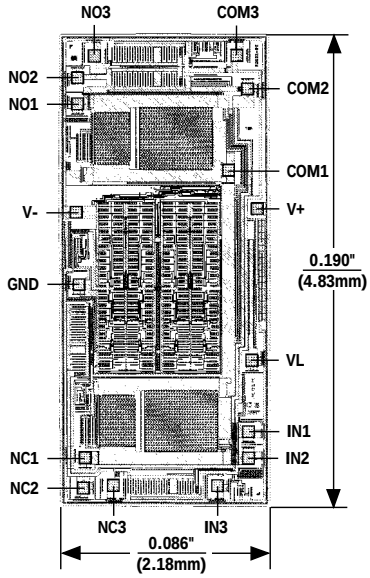
MAX4554



MAX4555



MAX4556



TRANSISTOR COUNT: 197

SUBSTRATE IS INTERNALLY CONNECTED TO V+

19-0448; Rev 0; 11/95

MAXIM

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

General Description

The MAX395 8-channel, serially controlled, single-pole/single-throw (SPST) analog switch offers eight separately controlled switches. The switches conduct equally well in either direction. On-resistance (100Ω max) is matched between switches to 5Ω max and is flat (10Ω max) over the specified signal range.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C.

Upon power-up, all switches are off, and the internal shift registers are reset to zero. The MAX395 is electrically equivalent to two MAX391 quad switches controlled by a serial interface, and is pin compatible with the MAX335.

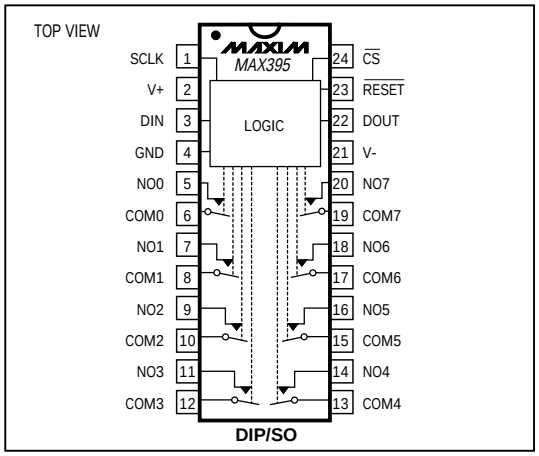
The serial interface is compatible with SPI™/QSPI™ and Microwire™. Functioning as a shift register, it allows data (at DIN) to be clocked in synchronously with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX395s to be daisy chained.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V supplies or a single +5V supply.

Applications

Serial Data-Acquisition Systems	Industrial and Process-Control Systems
Avionics	ATE Equipment
Audio Signal Routing	Networking

Pin Configuration



Features

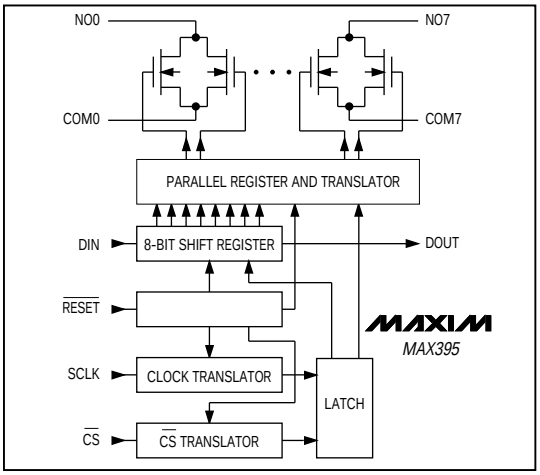
- ♦ **SPI™/QSPI™, Microwire™-Compatible Serial Interface**
- ♦ **8 Separately Controlled SPST Switches**
- ♦ **100Ω Signal Paths with ±5V Supplies**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **Asynchronous $\overline{\text{RESET}}$ Input**
- ♦ **Pin Compatible with Industry-Standard MAX335**
- ♦ **±2.7V to ±8V Dual Supplies +2.7V to +16V Single Supply**
- ♦ **>2kV ESD Protection per Method 3015.7**
- ♦ **TTL/CMOS-Compatible Inputs (with +5V or ±5V Supplies)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX395CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX395CWG	0°C to +70°C	24 Wide SO
MAX395C/D	0°C to +70°C	Dice*
MAX395ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX395EWG	-40°C to +85°C	24 Wide SO
MAX395MRG	-55°C to +125°C	24 Narrow CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
- V+ .....-0.3V, +17V
- V- .....-17V, +0.3V
- V+ to V-.....-0.3V, +17V
- SCLK, $\overline{CS}$, DIN, DOUT, $\overline{RESET}$ .....-0.3V to (V+ + 0.3V)
- NO, COM .....(V- - 2V) to (V+ + 2V)

Continuous Current into Any Terminal.....±30mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle).....±100mA

Continuous Power Dissipation (T_A = +70°C)
- Narrow Plastic DIP (derate 13.33mW/°C above +70°C)...1067mW
- Wide SO (derate 11.76mW/°C above +70°C).....941mW
- Narrow CERDIP (derate 12.50mW/°C above +70°C)....1000mW

Operating Temperature Ranges
- MAX395C_ G .....0°C to +70°C
- MAX395E_ G .....-40°C to +85°C
- MAX395MRG .....-55°C to +125°C

Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25°C		60	100	Ω
			C, E, M			125	
COM, NO On-Resistance Match Between Channels (Note 2)	ΔR_{ON}	V+ = 5V, V- = -5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25°C			5	Ω
			C, E, M			10	
COM, NO On-Resistance Flatness (Note 2)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V	T_A = +25°C			10	Ω
			C, E, M			15	
NO Off Leakage Current (Note 3)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM Off Leakage Current (Note 3)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = -4.5V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V- = -5.5V, V_{COM} = 4.5V, V_{NO} = -4.5V	T_A = +25°C	0.1	0.002	0.1	
			C, E, M	-10		10	
COM On Leakage Current (Note 3)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = V_{NO} = ±4.5V	T_A = +25°C	-0.2	0.01	0.2	nA
			C, E, M	-20		20	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
			C, E, M			500	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C	5	15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz	T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz	T_A = +25°C		2		pF
Switch On Capacitance	$C_{(ON)}$	V_{COM} = V_{NO} = GND, f = 1MHz	T_A = +25°C		8		pF
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	±3		±8	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C		7	20	µA
			C, E, M			30	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M	-2		2	

TIMING CHARACTERISTICS—Dual Supplies (Figure 1)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time	t_{CSH2}		C, E, M	240			ns
SCLK High Time	t_{CH}		C, E, M	190			ns
SCLK Low Time	t_{CL}		C, E, M	190			ns
Data Setup Time	t_{DS}		C, E, M	200	17		ns
Data Hold Time	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{NO} = 1mA	T_A = +25°C		125	175	Ω
			C, E, M			225	
NO Off Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	T_A = +25°C	-0.2	0.002	0.2	nA
			C, E, M	-20		20	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E, M	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E, M			0.8	V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E, M	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = -0.8mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = 1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
			C, E, M			500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
			C, E, M			500	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C		15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
V+, V- Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25°C		7	20	µA
			C, E, M			30	

TIMING CHARACTERISTICS—Single +5V Supply (Figure 1)

(V+ = +4.5V to +5.5V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Data Setup Time (Note 4)	t_{DS}		C, E, M	200	17		ns
Data Hold Time (Note 4)	t_{DH}		C, E, M	0	-17		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		85		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			100	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		70		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}		C, E, M	V-		V+	V
COM, NO On-Resistance	R_{ON}	V+ = 3.0V, V_{COM} = 1.5V, I_{NO} = 1mA	T_A = +25°C		270	500	Ω
			C, E, M			600	
NO Off Leakage Current (Notes 4, 5)	$I_{NO(OFF)}$	V+ = 3.0V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-5		5	
COM Off Leakage Current (Notes 4, 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	0.1	0.002	0.1	
			C, E, M	-5		5	
COM On Leakage Current (Notes 4, 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25°C	-0.1	0.002	0.1	nA
			C, E, M	-10		10	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25°C	-0.1	0.002	0.1	
			C, E, M	-10		10	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C, E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}		C, E			0.8	V
DIN, SCLK, $\overline{CS}$, Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.1mA	C, E, M	2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA	C, E, M	0		0.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		C, E, M		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		260	600	ns
			C, E, M			800	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	300	ns
			C, E, M			400	
Break-Before-Make Delay	t_{BBM}	From rising edge of $\overline{CS}$	T_A = +25°C		15		ns
Charge Injection (Note 4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC
Off Isolation (Note 6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		-90		dB
Channel-to-Channel Crosstalk (Note 7)	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25°C		<-90		dB
POWER SUPPLY							
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or 5V	T_A = +25°C		6	20	µA
			C, E, M			30	

TIMING CHARACTERISTICS—Single +3V Supply (Figure 1)

(V+ = +3.0V to +3.6V, V- = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SERIAL DIGITAL INTERFACE							
SCLK Frequency	f_{SCLK}		C, E, M	0		2.1	MHz
Cycle Time (Note 4)	$t_{CH} + t_{CL}$		C, E, M	480			ns
$\overline{CS}$ Lead Time (Note 4)	t_{CSS}		C, E, M	240			ns
$\overline{CS}$ Lag Time (Note 4)	t_{CSH2}		C, E, M	240			ns
SCLK High Time (Note 4)	t_{CH}		C, E, M	190			ns
SCLK Low Time (Note 4)	t_{CL}		C, E, M	190			ns
Data Setup Time (Note 4)	t_{DS}		C, E, M	200	38		ns
Data Hold Time (Note 4)	t_{DH}		C, E, M	0	-38		ns
DIN Data Valid after Falling SCLK (Note 4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25°C		150		ns
			C, E, M			400	
Rise Time of DOUT (Note 4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			300	ns
Allowable Rise Time at DIN, SCLK (Note 4)	t_{SCR}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
Fall Time of DOUT (Note 4)	t_{DF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			300	ns
Allowable Fall Time at DIN, SCLK (Note 4)	t_{SCF}	20% of V+ to 70% of V+, C_L = 10pF	C, E, M			2	µs
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25°C		105		ns

Note 1: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 2: $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 3: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.

Note 4: Guaranteed by design.

Note 5: Leakage testing at single supply is guaranteed by testing with dual supplies.

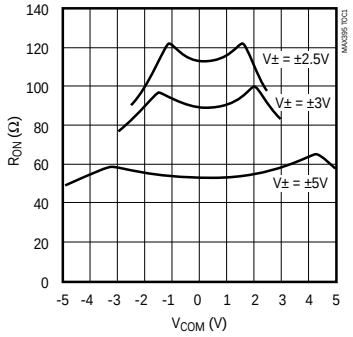
Note 6: See Figure 6. Off isolation = $20\log_{10} V_{COM}/V_{NO}$, V_{COM} = output. NO = input to off switch.

Note 7: Between any two switches. See Figure 3.

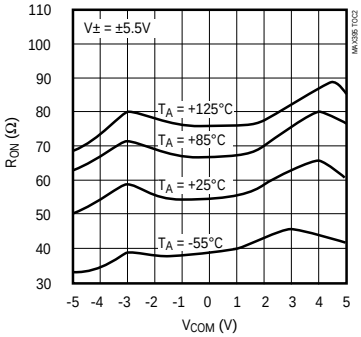
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

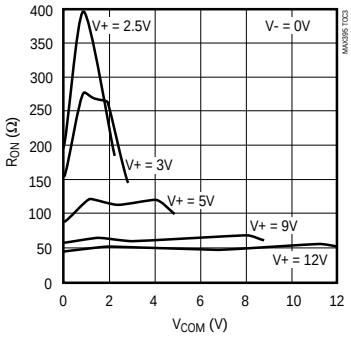
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



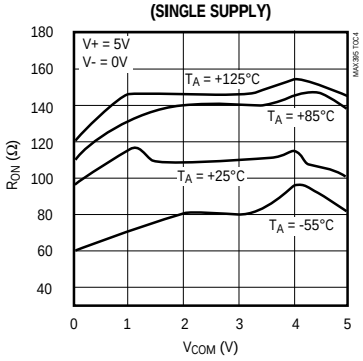
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



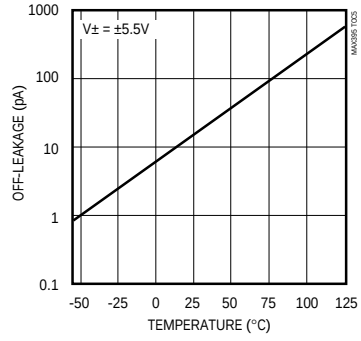
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



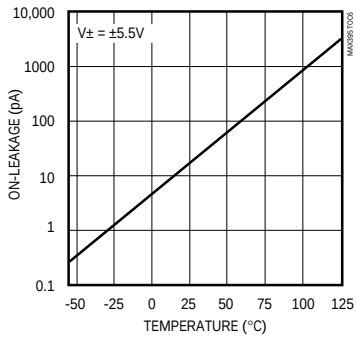
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



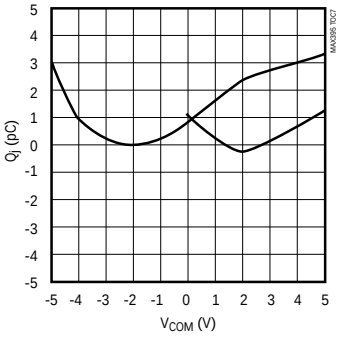
OFF-LEAKAGE vs. TEMPERATURE



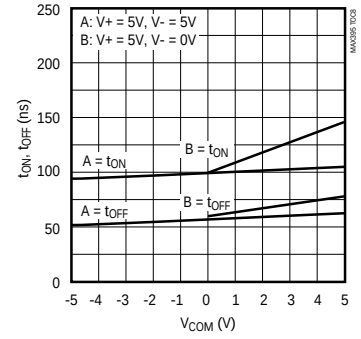
ON-LEAKAGE vs. TEMPERATURE



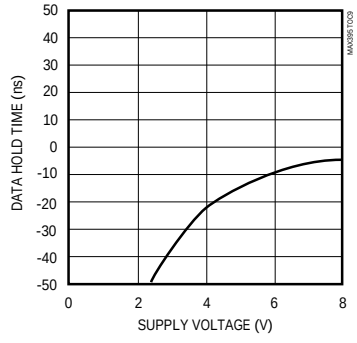
CHARGE INJECTION vs. V_{COM}



TURN-ON/OFF TIMES vs. V_{COM}



DATA HOLD TIME vs. POWER-SUPPLY VOLTAGE

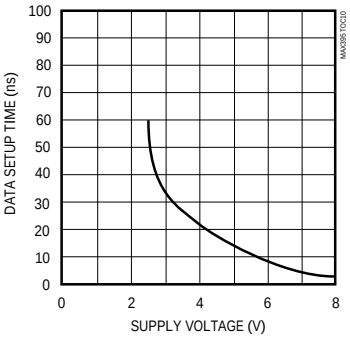


Serially Controlled, Low-Voltage, 8-Channel SPST Switch

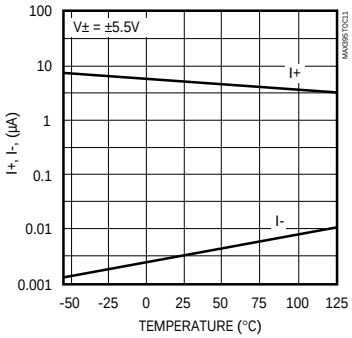
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

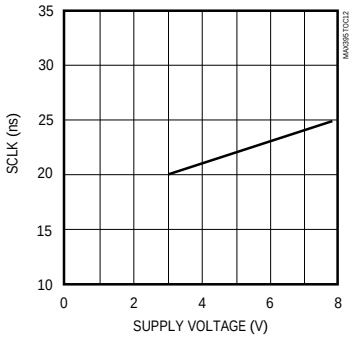
DATA SETUP TIME vs. POSITIVE SUPPLY VOLTAGE



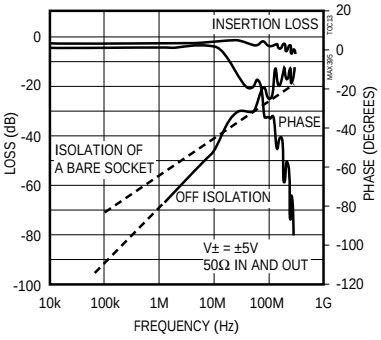
POWER-SUPPLY CURRENT vs. TEMPERATURE



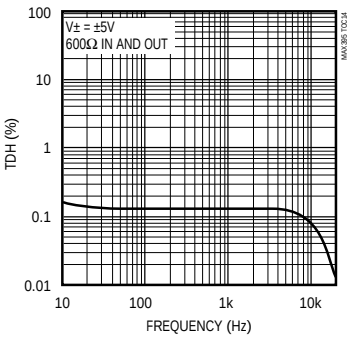
MINIMUM SCLK PULSE WIDTH vs. POSITIVE SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Digital Input
2	V+	Positive Analog Supply Voltage Input
3	DIN	Serial Data Digital Input
4	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
5, 7, 9, 11, 14, 16, 18, 20	NO0–NO7	Normally Open Analog Switches 0–7
6, 8, 10, 12, 13, 15, 17, 19	COM0–COM7	Common Analog Switches 0–7
21	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation
22	DOUT	Serial Data Digital Output. (High is sourced from V+.)
23	$\overline{\text{RESET}}$	Reset Input. Connect to digital (logic) supply (or V+). Drive low to set all switches off and set internal shift registers to 0.
24	$\overline{\text{CS}}$	Chip-Select Digital Input (Figure 1)

Note: NO_ and COM_ pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.

Detailed Description

Basic Operation

The MAX395's interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$ (Figure 2). While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronously with SCLK's rising edge. The data is an 8-bit word, each bit controlling one of eight switches in the MAX395 (Table 1). DOUT is the shift register's output, with data appearing synchronously with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their previous configuration. When the eight bits of data have been shifted in, $\overline{CS}$ is driven high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the first input bit (D7) at its output.

More or less than eight clock cycles can be entered during the $\overline{CS}$ low period. When this happens, the shift register will contain only the last eight serial data bits, regardless of when they were entered. On the rising edge of $\overline{CS}$, all the switches will be set to the corresponding states.

The MAX395's three-wire serial interface is compatible with SPI™, QSPI™, and Microwire™ standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX395 is considered a slave device (Figures 2 and 3). Upon power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state. This meets all the SPI and QSPI requirements.

Daisy Chaining

For a simple interface using several MAX395s, "daisy chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected together, and a stream of data is shifted through the MAX395s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX395 data chain.

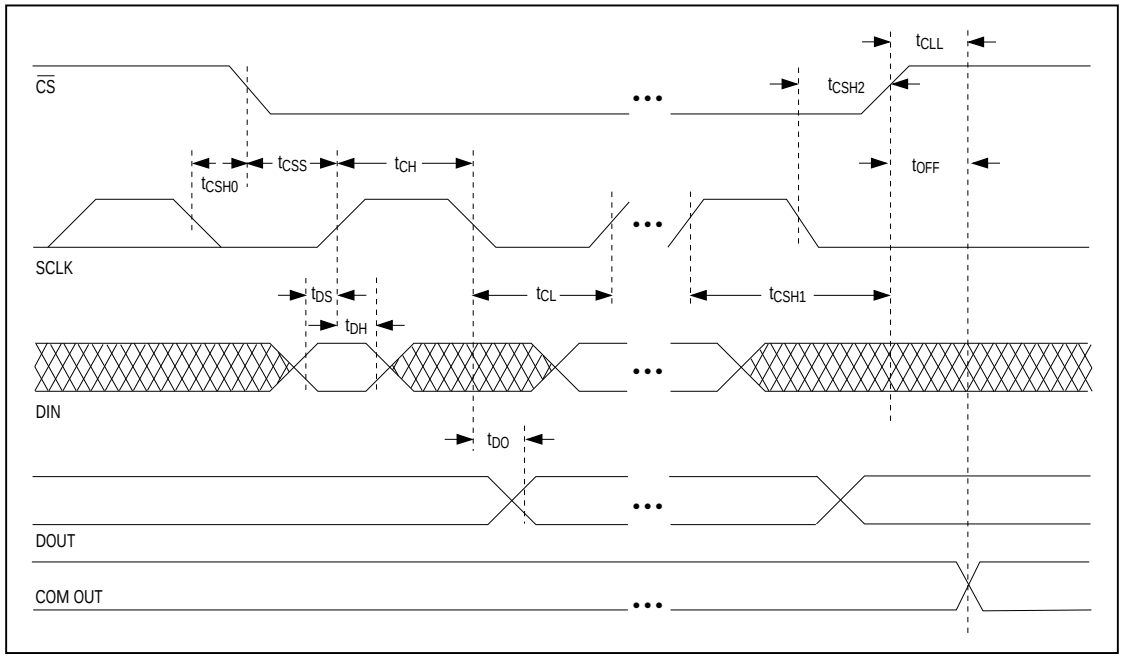


Figure 1. Timing Diagram

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

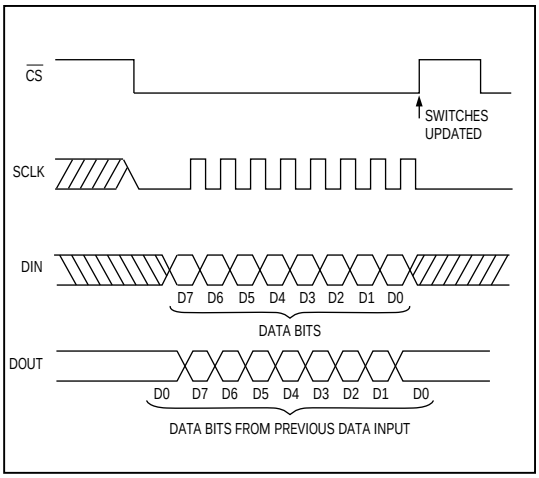


Figure 2. Three-Wire Interface Timing

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each decode logic individually control $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ pin is driven low, data is shifted in, and $\overline{CS}$ is driven high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Applications Information

Multiplexers

The MAX395 can be used as a multiplexer, but to obtain the same electrical performance with slightly improved programming speed, use the MAX349 8-channel mux or the MAX350 dual 4-channel mux, both in 18-pin packages.

Table 1. Serial-Interface Switch Programming

$\overline{RESET}$	DATA BITS								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	X	X	X	X	X	X	X	Switch 7 open (off)
1	1	X	X	X	X	X	X	X	Switch 7 closed (on)
1	X	0	X	X	X	X	X	X	Switch 6 open (off)
1	X	1	X	X	X	X	X	X	Switch 6 closed (on)
1	X	X	0	X	X	X	X	X	Switch 5 open (off)
1	X	X	1	X	X	X	X	X	Switch 5 closed (on)
1	X	X	X	0	X	X	X	X	Switch 4 open (off)
1	X	X	X	1	X	X	X	X	Switch 4 closed (on)
1	X	X	X	X	0	X	X	X	Switch 3 open (off)
1	X	X	X	X	1	X	X	X	Switch 3 closed (on)
1	X	X	X	X	X	0	X	X	Switch 2 open (off)
1	X	X	X	X	X	1	X	X	Switch 2 closed (on)
1	X	X	X	X	X	X	0	X	Switch 1 open (off)
1	X	X	X	X	X	X	1	X	Switch 1 closed (on)
1	X	X	X	X	X	X	X	0	Switch 0 open (off)
1	X	X	X	X	X	X	X	1	Switch 0 closed (on)

8x1 Multiplexer

To use the MAX395 as an 8x1 multiplexer, connect all common pins together (COM0–COM7) to form the mux output; the mux inputs are NO0–NO7.

The mux can be programmed normally, with only one channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse. In this mode, the channels are selected by sending a single high pulse (corresponding to the selected channel) at DIN, and a corresponding $\overline{CS}$ low pulse for every eight clock pulses. As this is clocked through the register by SCLK, each switch sequences one channel at a time, starting with Channel 7.

Dual, Differential 4-Channel Multiplexer

To use the MAX395 as a dual (4x2) mux, connect COM0–COM3 together and connect COM4–COM7 together, forming the two outputs. The mux input pairs become NO0/NO4, NO1/NO5, NO2/NO6, and NO3/NO7.

The mux can be programmed normally, with only one differential channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, the channels are selected by sending two high pulses spaced four clock pulses apart (corresponding to the two selected channels) at DIN, and a corresponding $\overline{CS}$ low pulse for each of the first eight clock pulses. As this is clocked through the register by

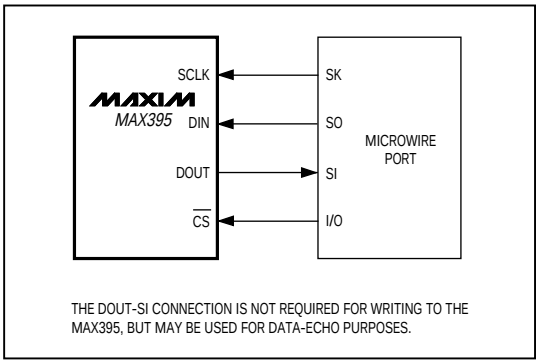


Figure 3. Connections for Microwire

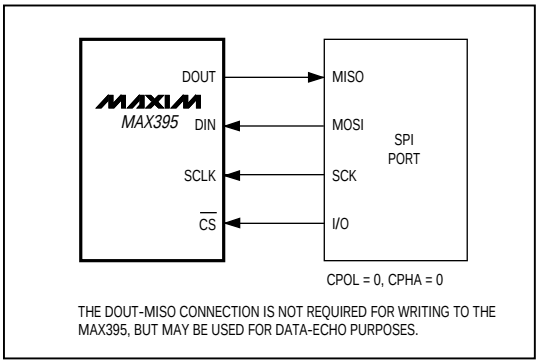


Figure 4. Connections for SPI and QSPI

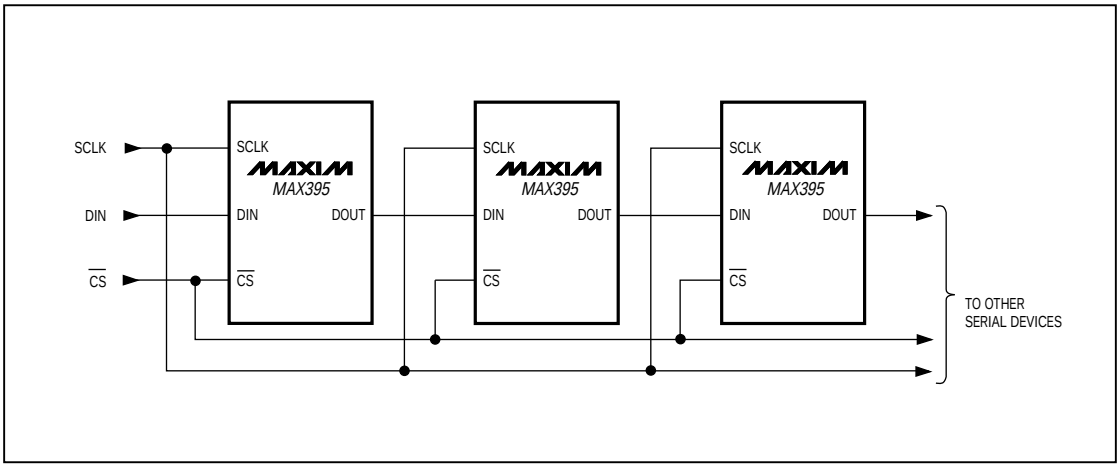


Figure 5. Daisy-Chained Connection

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

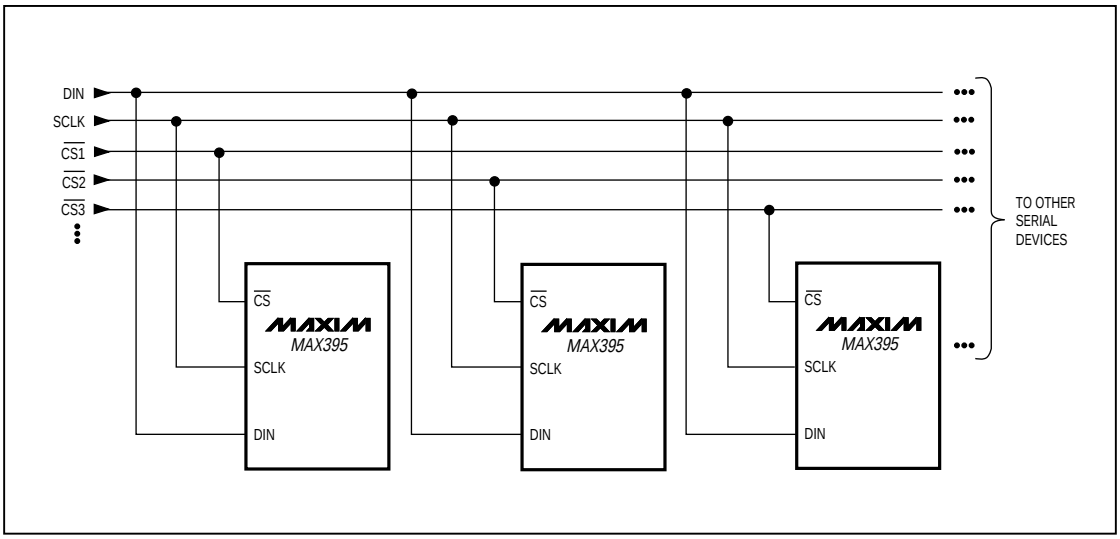


Figure 6. Addressable Serial Interface

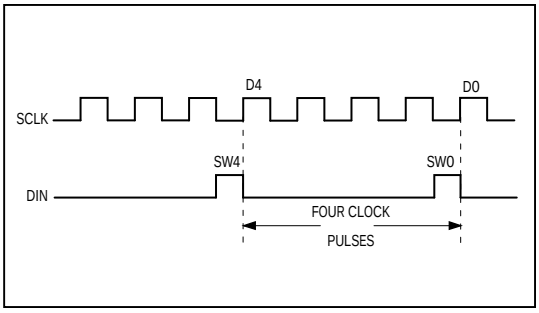


Figure 7. Differential Multiplexer Input Control

SCLK, each switch sequences one differential channel at a time, starting with channel 7/0. After the first eight bits have been sent, subsequent channel sequencing can occur by repeating this sequence or, even faster, by sending only one DIN high pulse and one $\overline{CS}$ low pulse for each four clock pulses.

SPDT Switches

To use the MAX395 as a quad, single-pole/double-throw (SPDT) switch, connect COM0 to NO1, COM2 to NO3, COM4 to NO5, and COM6 to NO7, forming the four "common" pins. Program these four switches with pairs of instructions, as shown in Table 2.

Reset Function

$\overline{RESET}$ is the internal reset pin. It is usually connected to a logic signal or V+. Drive $\overline{RESET}$ low to open all switches and set the contents of the internal shift register to zero simultaneously. When $\overline{RESET}$ is high, the part functions normally and DOUT is sourced from V+. $\overline{RESET}$ must not be driven beyond V+ or GND.

Power-Supply Considerations

Overview

The MAX395 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and to set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leak-

Table 2. SPDT Switch Programming

$\overline{RESET}$	DATA BITS								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	1	X	X	X	X	X	X	Switch 7 off and 6 on
1	1	0	X	X	X	X	X	X	Switch 6 off and 7 on
1	X	X	0	1	X	X	X	X	Switch 5 off and 4 on
1	X	X	1	0	X	X	X	X	Switch 4 off and 5 on
1	X	X	X	X	0	1	X	X	Switch 3 off and 2 on
1	X	X	X	X	1	0	X	X	Switch 2 off and 3 on
1	X	X	X	X	X	X	0	1	Switch 1 off and 0 on
1	X	X	X	X	X	X	1	0	Switch 0 off and 1 on

age current flows to the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+, and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly. So when V+ reaches +12V, the threshold is about 3.1V; slightly above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX395 operates with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 17V. **Do not connect the MAX395 V+ to +3V and connect the logic-level pins to TTL logic-level signals. This exceeds the absolute maximum ratings and can damage the part and/or external circuits.**

Single Supply

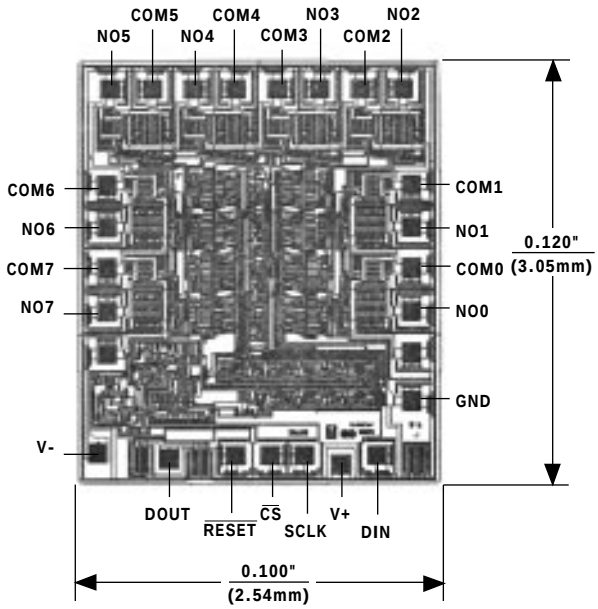
The MAX395 operates from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics)*. Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Serially Controlled, Low-Voltage, 8-Channel SPST Switch

Chip Topography



TRANSISTOR COUNT: 500

SUBSTRATE CONNECTED TO V+.

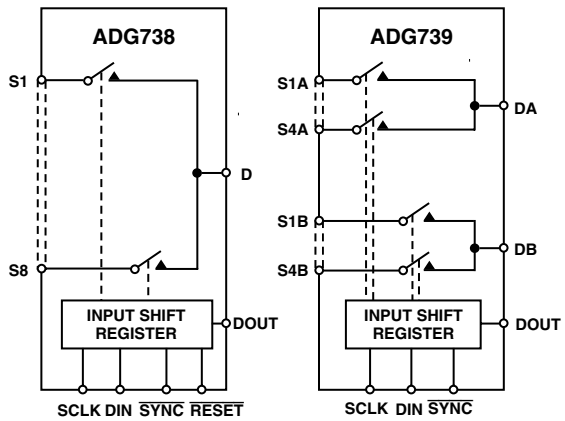
CMOS, Low-Voltage, 3-Wire Serially-Controlled, Matrix Switches

ADG738/ADG739

FEATURES
3-Wire Serial Interface
2.7 V to 5.5 V Single Supply
2.5 Ω On Resistance
0.75 Ω On-Resistance Flatness
100 pA Leakage Currents
Single 8-to-1 Multiplexer ADG738
Dual 4-to-1 Multiplexer ADG739
Power-On Reset
TTL/CMOS-Compatible

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG738 and ADG739 are CMOS analog matrix switches with a serially-controlled 3-wire interface. The ADG738 is an 8-channel matrix switch, while the ADG739 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range.

The ADG738 and ADG739 utilize a 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE™, and some DSP interface standards. The output of the shift register DOUT enables a number of these parts to be daisy-chained. On power-up, the internal shift register contains all zeros and all switches are in the OFF state.

Each switch conducts equally well in both directions when on, making these parts suitable for both multiplexing and demultiplexing applications. As each switch is turned on or off by a separate bit, these parts can also be configured as a type of switch array, where any, all, or none of the eight switches may be closed at any time. The input signal range extends to the supply rails.

All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG738 and ADG739 are available in 16-lead TSSOP packages.

PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. Single Supply Operation. The ADG738 and ADG739 are fully specified and guaranteed with 3 V and 5 V supply rails.
3. Low On Resistance, 2.5 Ω typical.
4. Any configuration of switches may be on or off at any one time.
5. Guaranteed Break-Before-Make Switching Action.
6. Small 16-lead TSSOP Package.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

REV. 0

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADG738/ADG739–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4.5	5	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±1	nA max	Test Circuit 3
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V/4.5 V, Test Circuit 4
	±0.1	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUT				
Output Low Voltage		0.4	max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	20		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		32	ns max	V_{S1} = 3 V
t_{OFF}	10		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		17	ns max	V_{S1} = 3 V
Break-Before-Make Time Delay, t_D	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_{S1} = V_{S8} = 3 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG738	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG739	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG738	85		pF typ	
ADG739	42		pF typ	
C_D, C_S (ON)				
ADG738	96		pF typ	
ADG739	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
Channels (ΔR_{ON})		1.2	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±1	nA max	Test Circuit 3
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 3 V/1 V, Test Circuit 4
	±0.1	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUT				
Output Low Voltage		0.4	max	I_{SINK} = 6 mA
C_{OUT}, Digital Output Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	40		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		70	ns max	V_{S1} = 2 V
t_{OFF}	14		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		25	ns max	V_{S1} = 2 V
Break-Before-Make Time Delay, t_D	12		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 2 V, Test Circuit 5
Charge Injection	±3		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 6
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz;
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
–3 dB Bandwidth				
ADG738	65		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 8
ADG739	100		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG738	85		pF typ	
ADG739	42		pF typ	
C_D, C_S (ON)				
ADG738	96		pF typ	
ADG739	48		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 3.3 V
		20	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 2.7 V to 5.5 V. All specifications –40°C to +85°C, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK Cycle Frequency
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK Active Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time
t_9[3]	20	ns min	SCLK Rising Edge to DOUT Valid

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]C_L = 20 pF, R_L = 1 kΩ.

Specifications subject to change without notice.

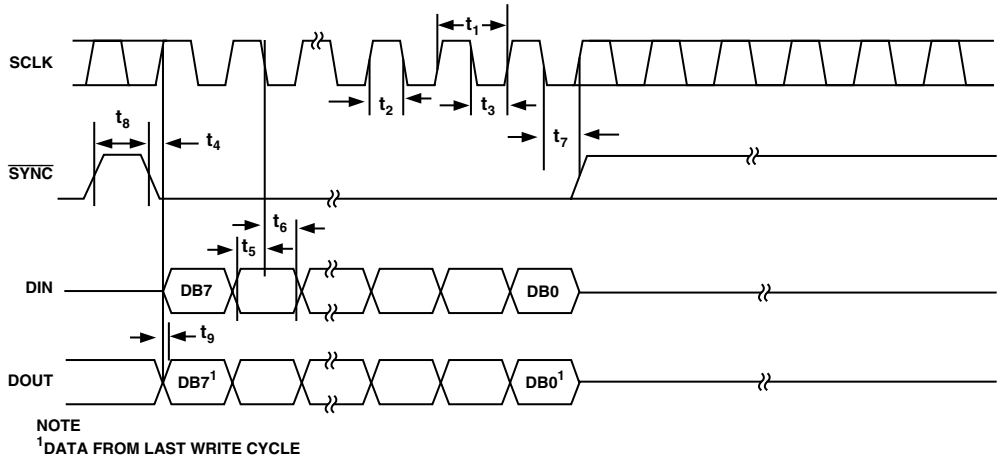
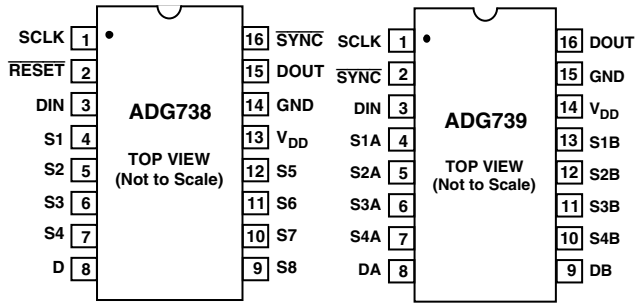


Figure 1. 3-Wire Serial Interface Timing Diagram

PIN FUNCTION DESCRIPTIONS

ADG738	ADG739	Mnemonic	Function
1	1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2		$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4, 5, 6, 7	4, 5, 6, 7	Sxx	Source. May be an input or output.
8	8, 9	Dx	Drain. May be an input or output.
9, 10, 11, 12	10, 11, 12, 13	Sxx	Source. May be an input or output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	15	GND	Ground Reference.
15	16	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output which should be pulled to the supply with an external resistor.
16	2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions.

PIN CONFIGURATIONS



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG738BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG739BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted.)

V_{DD} to GND ..... –0.3 V to +7 V
Analog, Digital Inputs[2] ..... –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D ..... 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, Each S ..... 30 mA
Continuous Current D, ADG739 ..... 80 mA
Continuous Current D, ADG738 ..... 120 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C

TSSOP Package
θ_{JA} Thermal Impedance ..... 150.4°C/W
θ_{JC} Thermal Impedance ..... 27.6°C/W
Lead Temperature, Soldering (10 seconds) ..... 300°C
IR Reflow, Peak Temperature ..... 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG738/ADG739 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
I_{DD}	Positive Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match Between any Two Channels, i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF."
I_D (OFF)	Drain Leakage Current with the Switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON."
V_{INL}	Maximum Input Voltage for Logic "0."
V_{INH}	Minimum Input Voltage for Logic "1."
I_{INL}(I_{INH})	Input Current of the Digital Input.
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
t_{ON}	Delay time between the 50% and 90% points of the $\overline{SYNC}$ rising edge and the switch "ON" condition.
t_{OFF}	Delay time between the 50% and 90% points of the $\overline{SYNC}$ rising edge and the switch "OFF" condition.
t_D	"OFF" time measured between the 80% points of both switches when switching from one switch to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3 dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

Typical Performance Characteristics–ADG738/ADG739

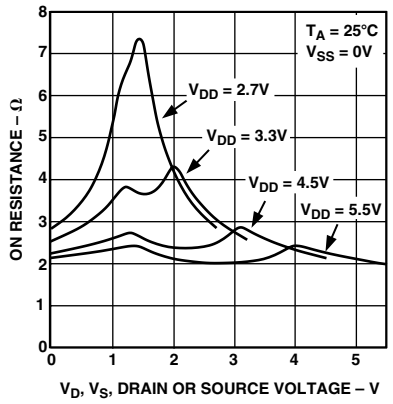


Figure 2. On Resistance as a Function of V_D (V_S)

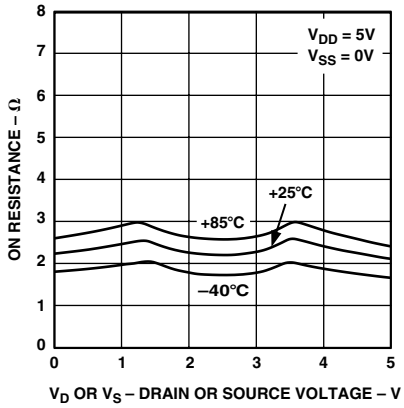


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures

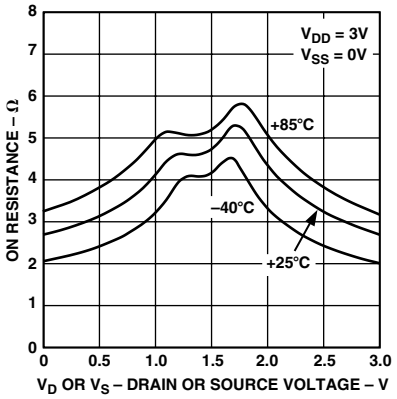


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures

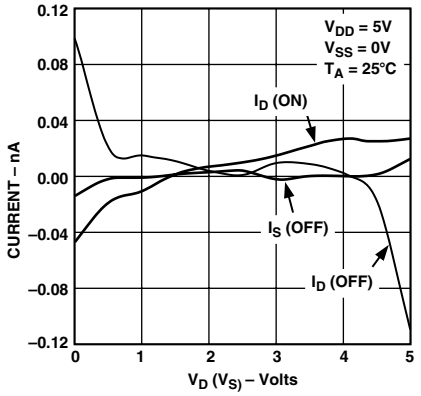


Figure 5. Leakage Currents as a Function of V_D (V_S)

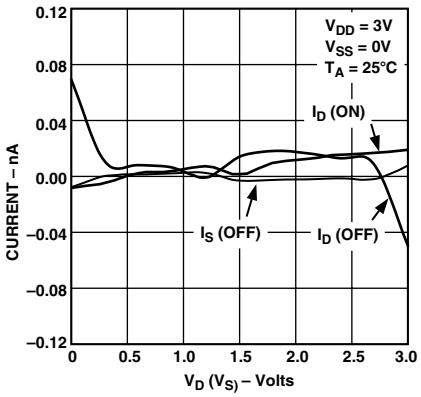


Figure 6. Leakage Currents as a Function of V_D (V_S)

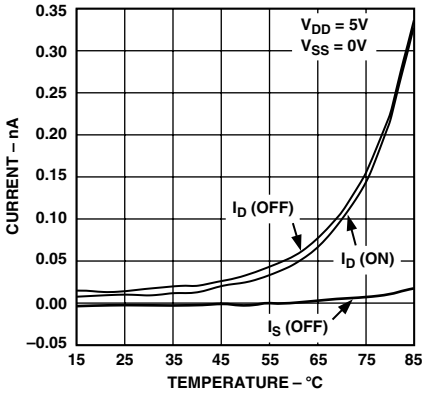


Figure 7. Leakage Currents as a Function of Temperature

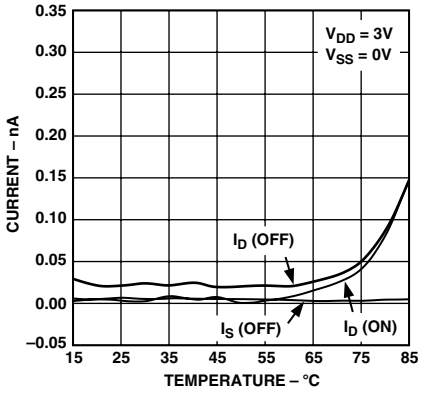


Figure 8. Leakage Currents as a Function of Temperature

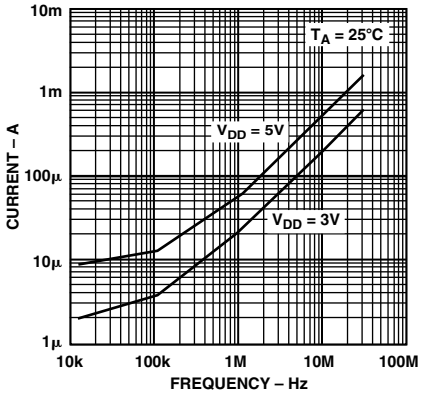


Figure 9. Input Currents vs. Switching Frequency

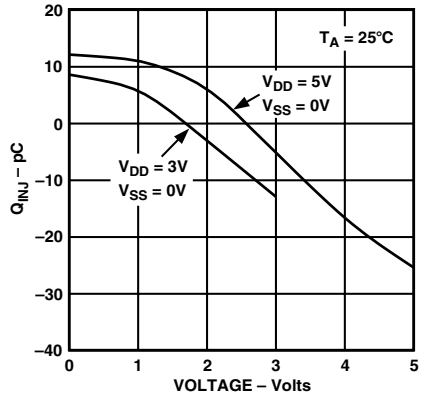


Figure 10. Charge Injection vs. Source Voltage

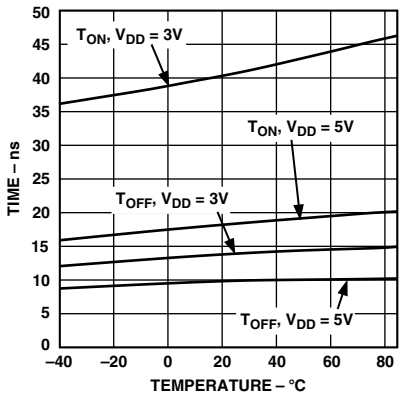


Figure 11. T_{ON}/T_{OFF} Times vs. Temperature

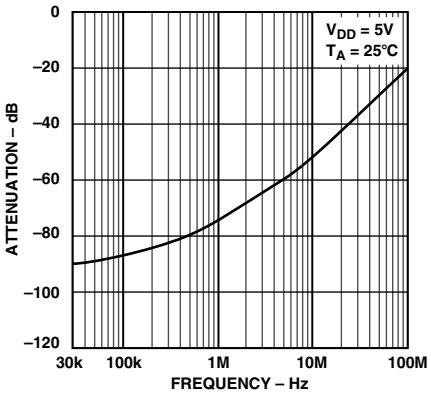


Figure 12. Off Isolation vs. Frequency

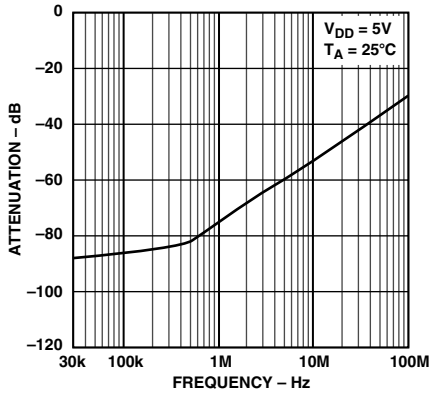


Figure 13. Crosstalk vs. Frequency

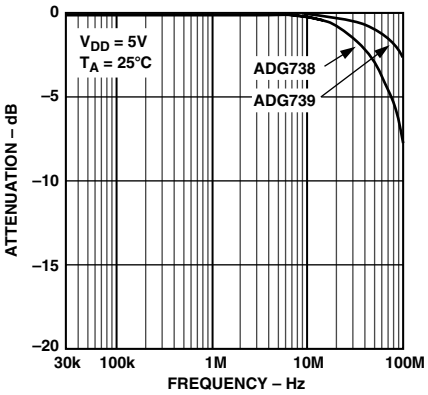


Figure 14. On Response vs. Frequency

GENERAL DESCRIPTION

The ADG738 and ADG739 are serially controlled, 8-channel and dual 4-channel Matrix Switches respectively. While providing the normal multiplexing and demultiplexing functions, these parts also provide the user with more flexibility as to where their signal may be routed. Each bit of the 8-bit serial word corresponds to one switch of the part. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. In order to minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the ON condition, and is required to stay ON, there will be minimal glitches on the output of the switch.

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG738 and ADG739 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{SYNC}$ and SCLK signals. Data may be written to the shift register in more or less than eight bits. In each case the shift register retains the last eight bits that were written.

When $\overline{SYNC}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on each falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 15 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy-chaining, delayed, of course, by eight bits. When all eight bits have been written into the shift register, the $\overline{SYNC}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{SYNC}$ held high, any further data or noise on the DIN line will have no effect on the shift register.

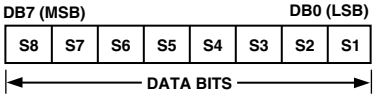


Figure 15. Input Shift Register Contents

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG738/ADG739 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG738/ADG739 requires an 8-bit data word with data valid on the falling edge of SCLK.

Data from the previous write cycle is available on the DOUT pin. The following figures illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

ADSP-21xx to ADG738/ADG739

An interface between the ADG738/ADG739 and the ADSP-21xx is shown in Figure 16. In the interface example shown, SPORT0 is used to transfer data to the Matrix Switch. The SPORT control register should be configured as follows: internal Clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the Matrix Switch. The update of each switch condition takes place automatically when $\overline{TFS}$ is taken high.

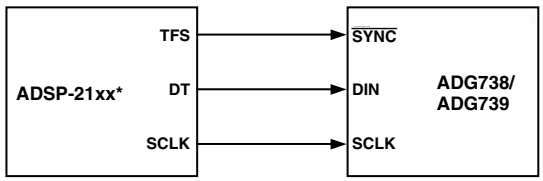


Figure 16. ADSP-21xx to ADG738/ADG739 Interface

8051 Interface to ADG738/ADG739

A serial interface between the ADG738/ADG739 and the 8051 is shown in Figure 17. TXD of the 8051 drives SCLK of the ADG738/ADG739, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user will have to ensure that the data in the SBUF register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the Matrix Switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between the ADG738/ADG739 and microcontroller interface.

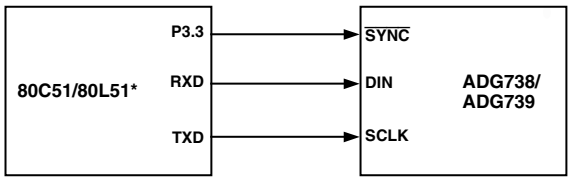


Figure 17. 8051 Interface to ADG738/ADG739

MC68HC11 Interface to ADG738/ADG739

Figure 18 shows an example of a serial interface between the ADG738/ADG739 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the Matrix Switch, while the MOSI output drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case PC7.

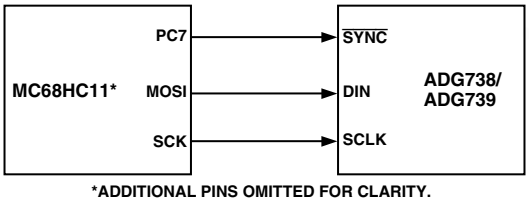


Figure 18. MC68HC11 Interface to ADG738/ADG739

The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0 and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

If the user wishes to verify the data previously written to the input shift register, the DOUT line could be connected to MISO of the MC68HC11, and with $\overline{\text{SYNC}}$ low, the shift register would clock data out on the rising edges of SCLK.

APPLICATIONS

Expand the Number of Selectable Serial Devices Using an ADG739

The dual 4-channel ADG739 multiplexer can be used to multiplex a single chip select line in order to provide chip selects for up to four devices on the SPI bus. Figure 19 illustrates the ADG739 in such a typical configuration. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is a serially controlled device also. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus will be enabled and data will be clocked into its shift register on the falling edges of SCLK. The convenient design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices need to be addressed via one chip select line, the ADG738 is an 8-channel device and would allow further expansion of the chip select scheme. There may be some digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock will minimize the effects of digital feedthrough on the analog channels.

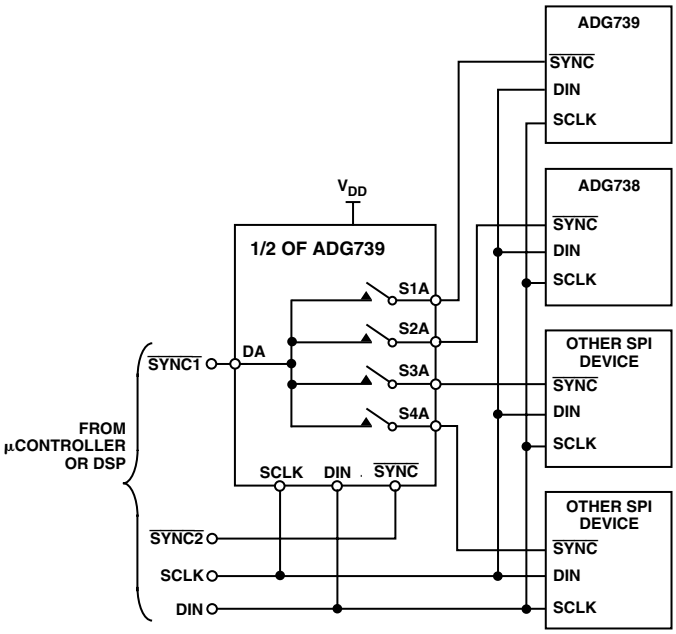


Figure 19. Addressing Multiple Serial Devices Using an ADG739

Daisy-Chaining Multiple ADG738s

A number of ADG738 matrix switches may be daisy-chained simply by using the DOUT pin. DOUT is an open drain output that should be pulled to the supply with an external resistor. Figure 20 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three parts in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all parts are enabled, data is written to the parts via DIN, and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high and all switches are updated simultaneously. Further shift registers may be added in series.

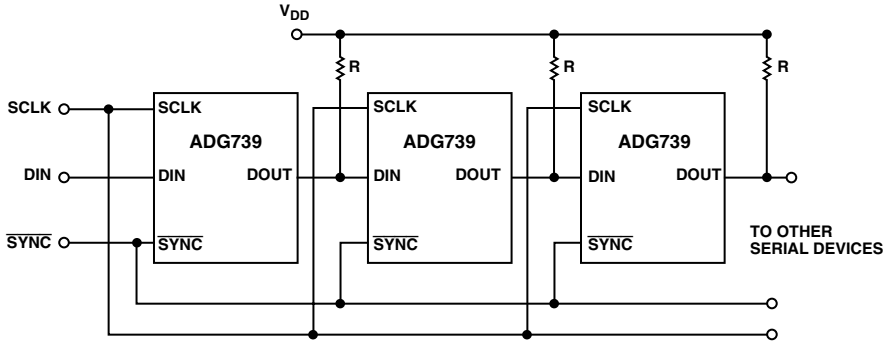
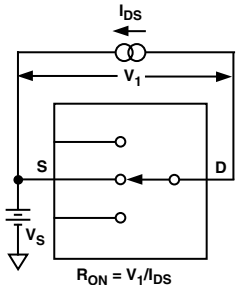
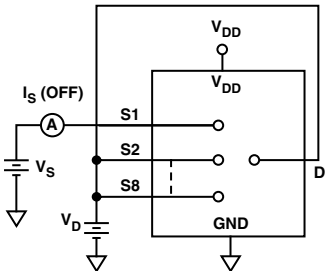


Figure 20. Multiple ADG739 Devices in a Daisy-Chained Configuration

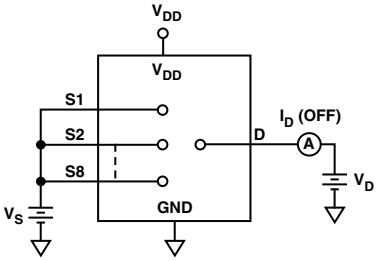
TEST CIRCUITS



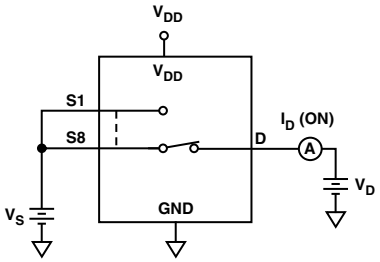
Test Circuit 1. On Resistance



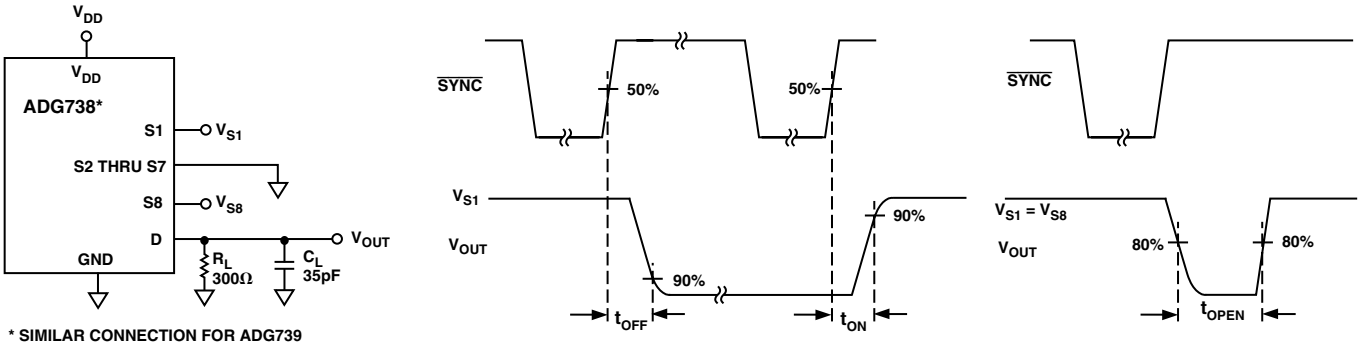
Test Circuit 3. I_S (OFF)



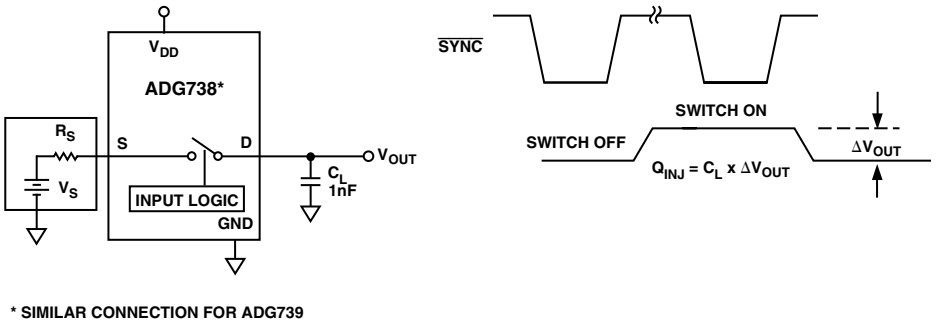
Test Circuit 2. I_D (OFF)



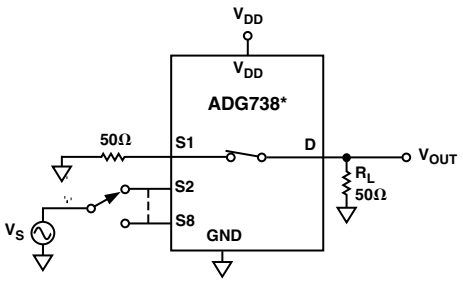
Test Circuit 4. I_D (ON)



Test Circuit 5. Switching Times and Break-Before-Make Times



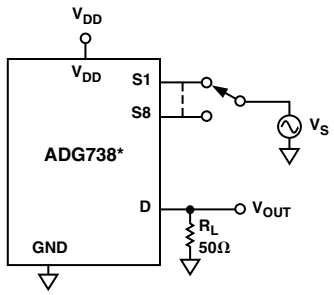
Test Circuit 6. Charge Injection



* SIMILAR CONNECTION FOR ADG739

CHANNEL-TO-CHANNEL CROSSTALK = $20LOG_{10}(V_{OUT}/V_S)$

Test Circuit 7. Channel-to-Channel Crosstalk



*SIMILAR CONNECTION FOR ADG739

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20LOG_{10}(V_{OUT}/V_S)$

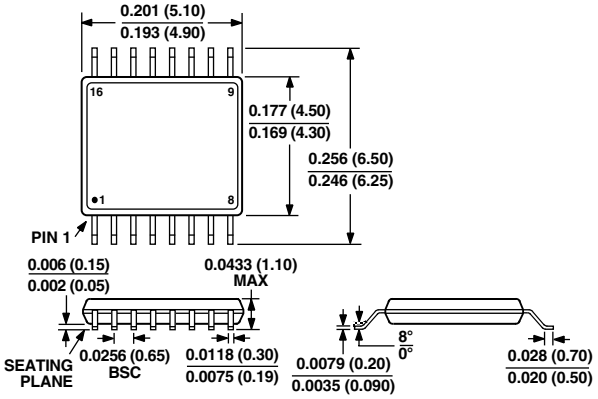
INSERTION LOSS = $20LOG_{10}\left(\frac{V_{OUT}\text{ WITH SWITCH}}{V_{OUT}\text{ WITHOUT SWITCH}}\right)$

Test Circuit 8. Off Isolation and Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)



C3834–8–4/00 (rev. 0) 01003

PRINTED IN U.S.A.

16-/32-Channel, Serially Controlled 4 Ω 1.8 V to 5.5 V, ±2.5 V, Analog Multiplexers

ADG725/ADG731

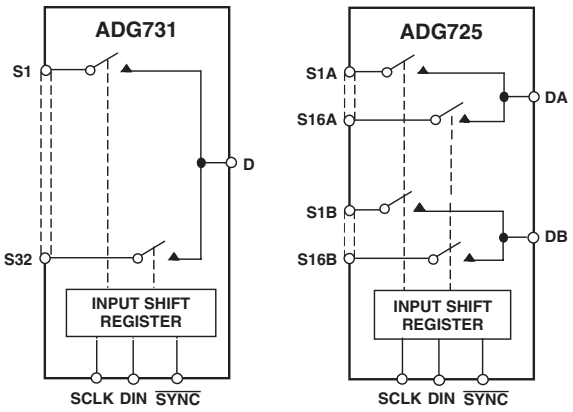
FEATURES

- 3-Wire SPI Compatible Serial Interface
- 1.8 V to 5.5 V Single Supply
- ±2.5 V Dual-Supply Operation
- 4 Ω On Resistance
- 0.5 Ω On Resistance Flatness
- 7 mm x 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package
- Rail-to-Rail Operation
- Power-On Reset
- 42 ns Switching Times
- Single 32-to-1 Channel Multiplexer
- Dual/Differential 16-to-1 Channel Multiplexer
- TTL/CMOS Compatible Inputs
- For Functionally Equivalent Devices with Parallel Interface, See ADG726/ADG732

APPLICATIONS

- Optical Applications
- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems
- Medical Instrumentation
- Automatic Test Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG731/ADG725 are monolithic, CMOS, 32-channel/dual 16-channel analog multiplexers with a serially controlled 3-wire interface. The ADG731 switches one of 32 inputs (S1–S32) to a common output, D. The ADG725 can be configured as a dual mux switching one of 16 inputs to one output, or a differential mux switching one of 16 inputs to a differential output.

These mulitplexers utilize a 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and some DSP interface standards. On power-up, the Internal Shift Register contains all zeros and all switches are in the OFF state.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed with very low on resistance and leakage currents. They operate from a single supply of 1.8 V to 5.5 V or a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms, is closely matched between switches, and is very flat over the full signal range.

These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG731 and ADG725 are serially controlled 32-channel, and dual/differential 16-channel multiplexers, respectively. They are available in either a 48-lead LFCSP or TQFP package.

PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. 1.8 V to 5.5 V Single-Supply or ±2.5 V Dual-Supply Operation. These parts are specified and guaranteed with 5 V ±10%, 3 V ±10% single-supply, and ±2.5 V ±10% dual-supply rails.
3. On Resistance of 4 Ω.
4. Guaranteed Break-Before-Make Switching Action.
5. 7 mm × 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADG725/ADG731–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match between		0.3	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = 1 V or 4.5 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	42		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	53	62	ns max	V_{S1} = 3 V/0 V, V_{S32} = 0 V/3 V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 3 V; Test Circuit 6
Charge Injection	5		pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	170		pF typ	f = 1 MHz
ADG731	340		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	175		pF typ	f = 1 MHz
ADG731	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	7		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On Resistance Match between		0.35	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω max	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±1	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_S = V_D = 1 V or 3 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	60		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	80	90	ns max	V_{S1} = 2 V/0 V, V_{S32} = 0 V/2 V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 2 V; Test Circuit 6
Charge Injection	1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	15		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	170		pF typ	f = 1 MHz
ADG731	340		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	175		pF typ	f = 1 MHz
ADG731	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	5		μA typ	Digital Inputs = 0 V or 3.3 V
		10	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

DUAL-SUPPLY SPECIFICATIONS[1] (V_{DD} = +2.5 V ± 10%, V_{SS} = –2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match Between		0.3	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = –2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V;
	±0.25	±0.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +2.25 V/–1.25 V; Test Circuit 4
ADG725	±0.5	±2.5	nA max	
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	55		ns typ	R_L = 300 Ω, C_L = 35 pF; Test Circuit 5
	75	84	ns max	V_{S1} = 1.5 V/0 V, V_{S32} = 0 V/1.5 V
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 1.5 V; Test Circuit 6
Charge Injection	1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG725	130		pF typ	f = 1 MHz
ADG731	260		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	150		pF typ	f = 1 MHz
ADG731	300		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +2.75 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 2.75 V
		20	μA max	
I_{SS}	10		μA typ	V_{SS} = –2.75 V
		20	μA max	Digital Inputs = 0 V or 2.75 V

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK Cycle Frequency
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_5	40	ns min	Minimum $\overline{SYNC}$ Low Time
t_6	5	ns min	Data Setup Time
t_7	4.5	ns min	Data Hold Time
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
Specifications subject to change without notice.

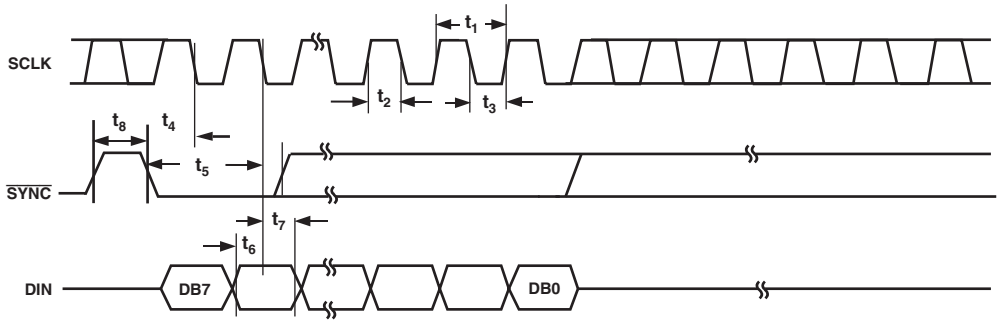


Figure 1. 3-Wire Serial Interface Timing Diagram

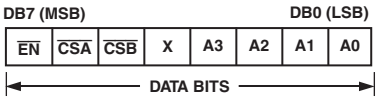


Figure 2. ADG725 Input Shift Register Contents

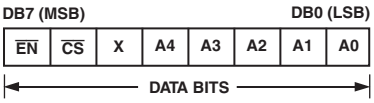


Figure 3. ADG731 Input Shift Register Contents

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to V_{SS} . . . . . 7 V
V_{DD} to GND . . . . . –0.3 V to +7 V
V_{SS} to GND . . . . . +0.3 V to –7 V
Analog Inputs[2] . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 60 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Thermal Impedance (4-Layer Board)
48-lead LFCSP . . . . . 25°C/W
48-lead TQFP . . . . . 54.6°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature (<20 seconds) . . . . . 235°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at SCLK, $\overline{\text{SYNC}}$, DIN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

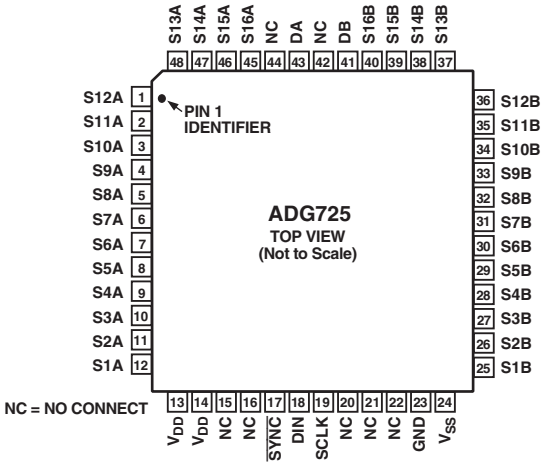
Model	Temperature Range	Package Description	Package Option
ADG725BCP	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BCP-REEL	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BCP-REEL7	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG725BSU	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG725BSU-REEL	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG731BCP	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BCP-REEL	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BCP-REEL7	–40°C to +85°C	Lead Frame Chip-Scale Package (LFCSP)	CP-48
ADG731BSU	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48
ADG731BSU-REEL	–40°C to +85°C	Thin Plastic Quad Flat Package (TQFP)	SU-48

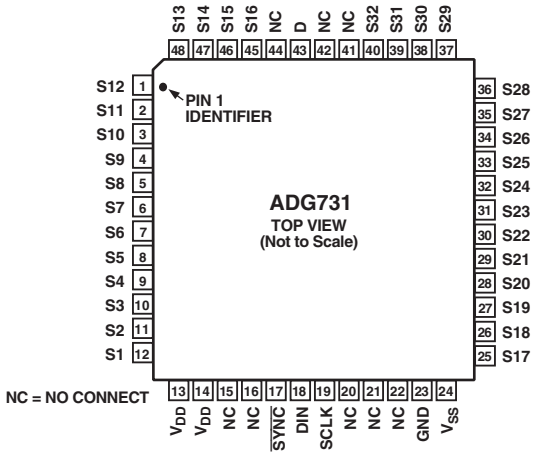
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG725/ADG731 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

48-Lead LFCSP and TQFP





PIN FUNCTION DESCRIPTIONS

ADG725	ADG731	Mnemonic	Function
1–12, 25–40, 45–48	1–12, 25–40, 45–48	Sxx	Source. May be an input or output.
13, 14	13, 14	V_{DD}	Power Supply Input. These parts can be operated from a single supply of 1.8 V to 5.5 V and a dual supply of ±2.5 V.
17	17	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input Shift Register is enabled. An 8-bit counter is also enabled. Data is transferred on the falling edges of the following clocks. After eight falling clock edges, switch conditions are automatically updated. $\overline{SYNC}$ may be used to frame the signal or just pulled low for a short period of time to enable the counter and input buffers.
18	18	DIN	Serial Data Input. Data is clocked into the 8-bit Input Register MSB first on the falling edge of the serial clock input.
19	19	SCLK	Serial Clock Input. Data is clocked into the Input Shift Register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
23	23	GND	Ground Reference
24	24	V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND.
41, 43	N/A	DA, DB	Drain. May be an input or output.
N/A	43	D	Drain. May be an input or output.

Table I. ADG725 Truth Table

A3	A2	A1	A0	$\overline{EN}$	$\overline{CSA}$	$\overline{CSB}$	Switch Condition
X	X	X	X	X	1	1	Retains Previous Switch Condition
X	X	X	X	1	X	X	All Switches OFF
0	0	0	0	0	0	0	S1A – DA, S1B – DB
0	0	0	1	0	0	0	S2A – DA, S2B – DB
0	0	1	0	0	0	0	S3A – DA, S3B – DB
0	0	1	1	0	0	0	S4A – DA, S4B – DB
0	1	0	0	0	0	0	S5A – DA, S5B – DB
0	1	0	1	0	0	0	S6A – DA, S6B – DB
0	1	1	0	0	0	0	S7A – DA, S7B – DB
0	1	1	1	0	0	0	S8A – DA, S8B – DB
1	0	0	0	0	0	0	S9A – DA, S9B – DB
1	0	0	1	0	0	0	S10A – DA, S10B – DB
1	0	1	0	0	0	0	S11A – DA, S11B – DB
1	0	1	1	0	0	0	S12A – DA, S12B – DB
1	1	0	0	0	0	0	S13A – DA, S13B – DB
1	1	0	1	0	0	0	S14A – DA, S14B – DB
1	1	1	0	0	0	0	S15A – DA, S15B – DB
1	1	1	1	0	0	0	S16A – DA, S16B – DB

X = Don't Care

Table II. ADG731 Truth Table

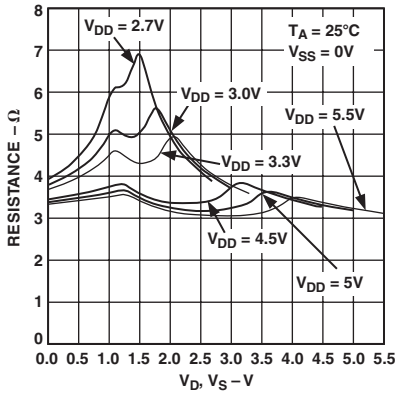
A4	A3	A2	A1	A0	$\overline{EN}$	$\overline{CSA}$	Switch Condition
X	X	X	X	X	X	1	Retains Previous Switch Condition
X	X	X	X	X	1	X	All Switches OFF
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	2
0	0	0	1	0	0	0	3
0	0	0	1	1	0	0	4
0	0	1	0	0	0	0	5
0	0	1	0	1	0	0	6
0	0	1	1	0	0	0	7
0	0	1	1	1	0	0	8
0	1	0	0	0	0	0	9
0	1	0	0	1	0	0	10
0	1	0	1	0	0	0	11
0	1	0	1	1	0	0	12
0	1	1	0	0	0	0	13
0	1	1	0	1	0	0	14
0	1	1	1	0	0	0	15
0	1	1	1	1	0	0	16
1	0	0	0	0	0	0	17
1	0	0	0	1	0	0	18
1	0	0	1	0	0	0	19
1	0	0	1	1	0	0	20
1	0	1	0	0	0	0	21
1	0	1	0	1	0	0	22
1	0	1	1	0	0	0	23
1	0	1	1	1	0	0	24
1	1	0	0	0	0	0	25
1	1	0	0	1	0	0	26
1	1	0	1	0	0	0	27
1	1	0	1	1	0	0	28
1	1	1	0	0	0	0	29
1	1	1	0	1	0	0	30
1	1	1	1	0	0	0	31
1	1	1	1	1	0	0	32

X = Don't Care

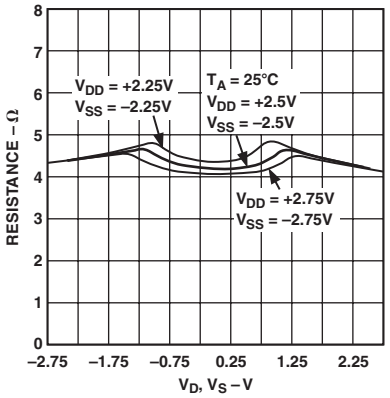
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
V_D (V_S)	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match between any Two Channels.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch OFF.
I_D (OFF)	Drain Leakage Current with the Switch OFF.
I_D, I_S (ON)	Channel Leakage Current with the Switch ON.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
I_{INL} (I_{INH})	Input Current of the Digital Input.
C_S (OFF)	OFF Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	OFF Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	ON Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
$t_{TRANSITION}$	Delay time measured between the 50% points of the eighth clock falling edge and 90% points of the output when switching from one address state to another.
t_D	OFF time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
OFF Isolation	A measure of unwanted signal coupling through an OFF switch.
Crosstalk	A measure of unwanted signal is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency Response of the ON Switch.
Insertion Loss	The Loss Due to the On Resistance of the Switch.

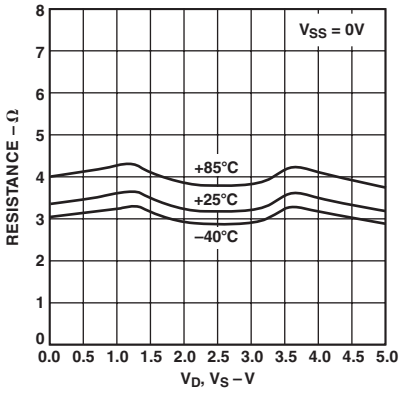
ADG725/ADG731–Typical Performance Characteristics



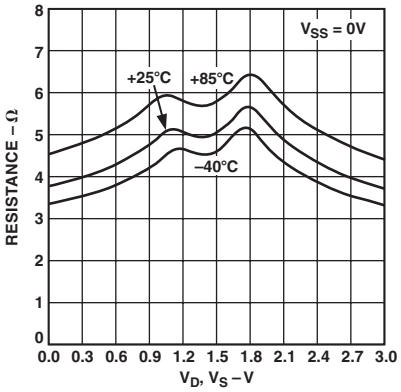
TPC 1. On Resistance vs. V_D (V_S), Single Supply



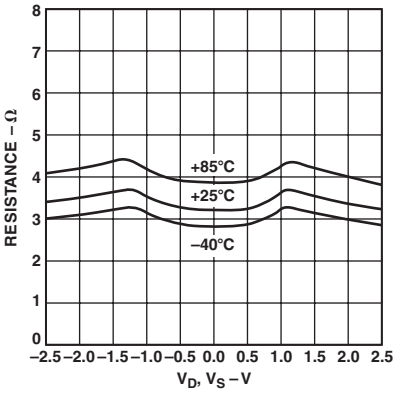
TPC 2. On Resistance vs. V_D (V_S), Dual Supply



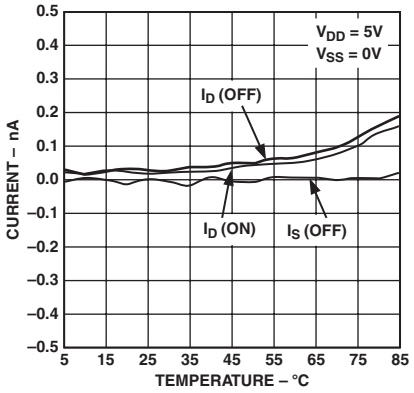
TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply



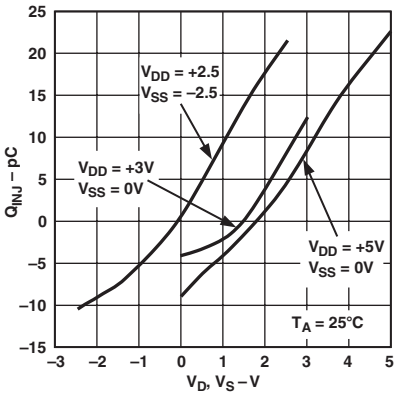
TPC 4. On Resistance vs. V_D (V_S), Single Supply



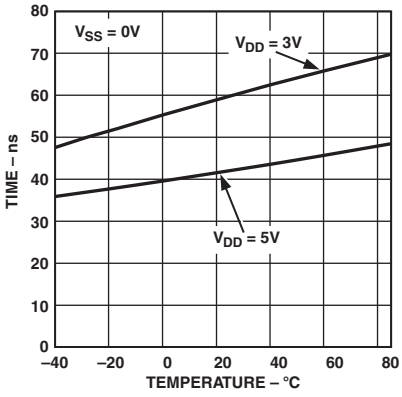
TPC 5. On Resistance vs. V_D (V_S), Dual Supply



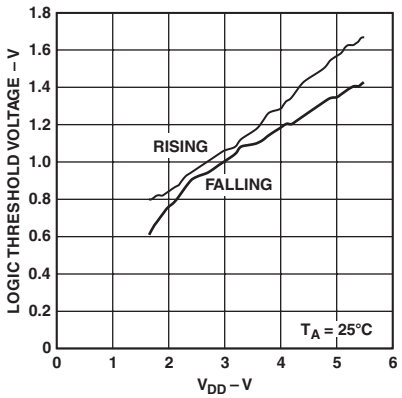
TPC 6. Leakage Currents vs. Temperature



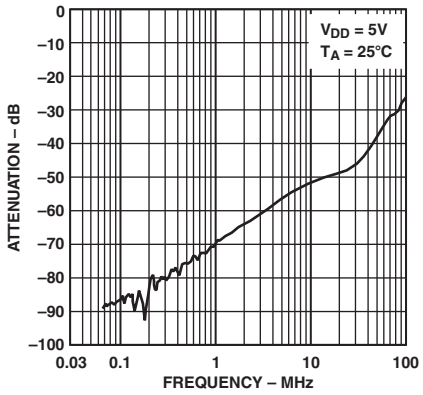
TPC 7. ADG731 Charge Injection vs. Source Voltage



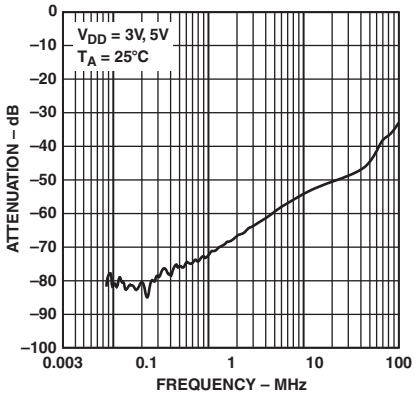
TPC 8. Switching Times vs. Temperature



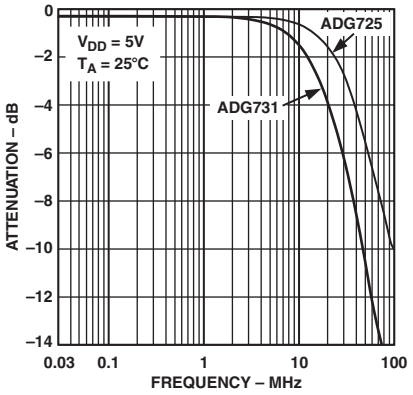
TPC 9. Logic Threshold Voltage vs. Supply Voltage



TPC 10. OFF Isolation vs. Frequency

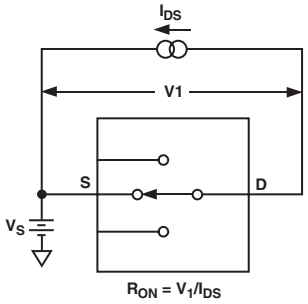


TPC 11. Crosstalk vs. Frequency

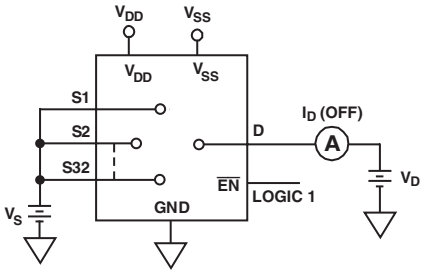


TPC 12. ON Response vs. Frequency

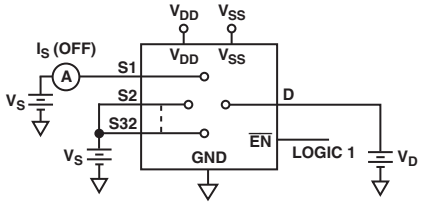
Test Circuits



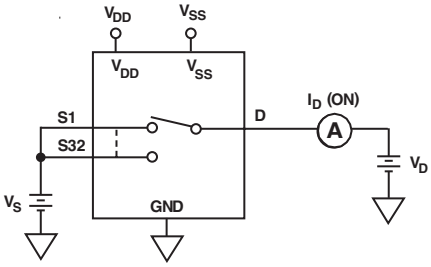
Test Circuit 1. On Resistance



Test Circuit 3. I_D (OFF)

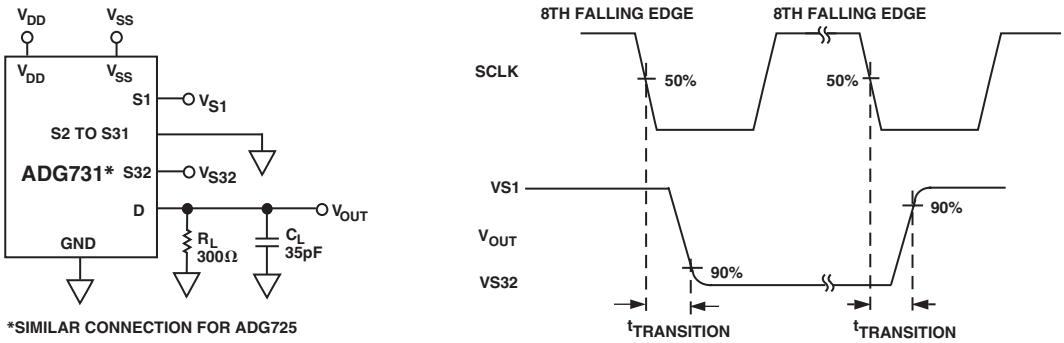


Test Circuit 2. I_S (OFF)

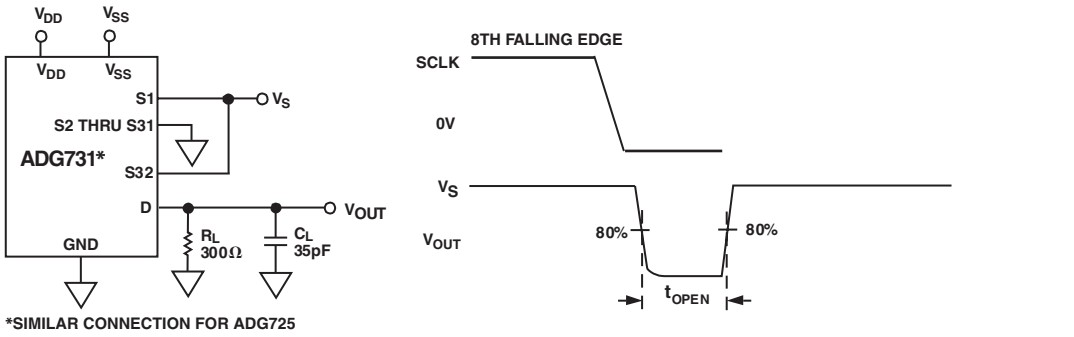


Test Circuit 4. I_D (ON)

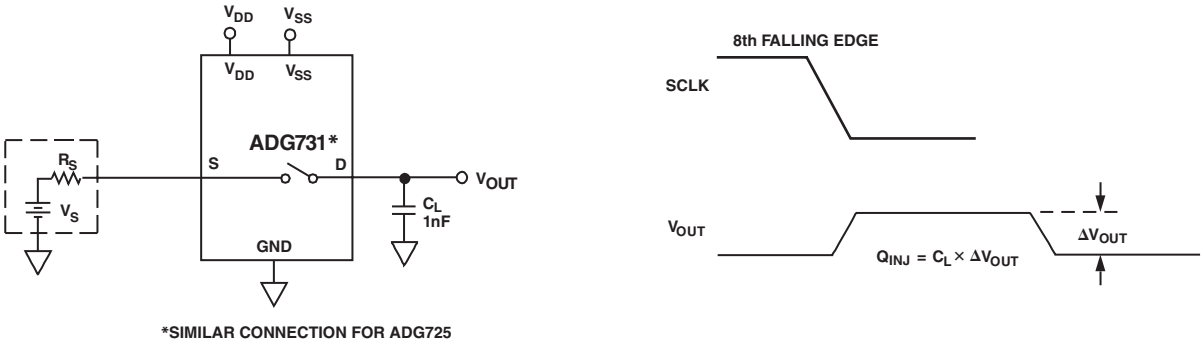
TEST CIRCUITS (continued)



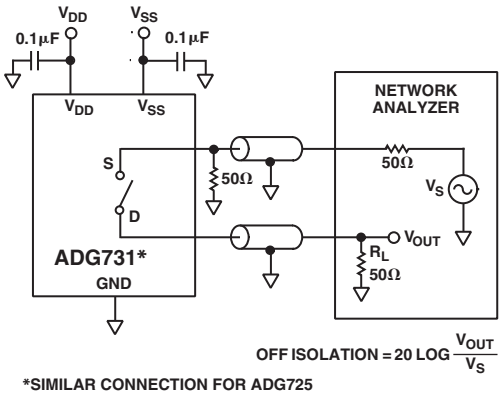
Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$



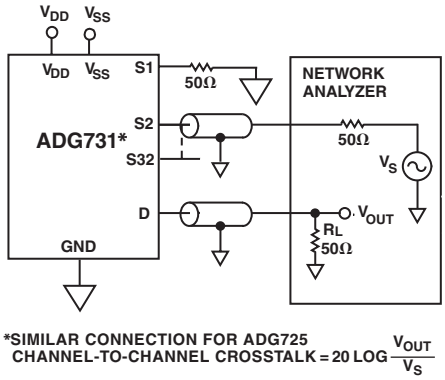
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



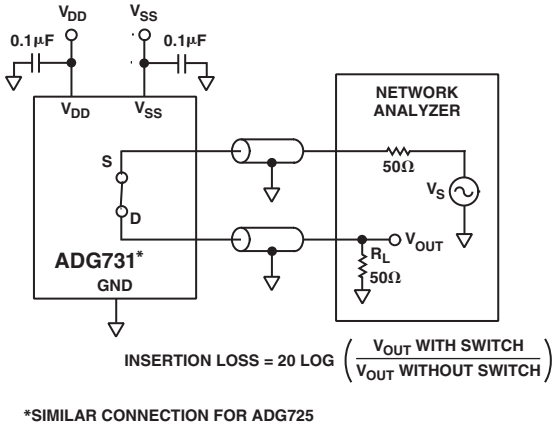
Test Circuit 7. Charge Injection



Test Circuit 8. OFF Isolation



Test Circuit 9. Channel-to-Channel Crosstalk



Test Circuit 10. Bandwidth

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition. The Internal Shift Register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG725 and ADG731 have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit Shift Register via DIN under the control of the $\overline{\text{SYNC}}$ and SCLK signals.

When $\overline{\text{SYNC}}$ goes low, the Input Shift Register is enabled. An 8-bit counter is also enabled. Data from DIN is clocked into the Shift Register on the falling edge of SCLK. Figures 2 and 3 show the contents of the Input Shift Registers for these devices. When the part has received eight clock cycles after $\overline{\text{SYNC}}$ has been pulled low, the switches are automatically updated with the new configuration and the Input Shift Register is disabled.

The ADG725 $\overline{\text{CSA}}$ and $\overline{\text{CSB}}$ data bits allow the user the flexibility to change the configuration of either or both banks of the multiplexer.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG725/ADG731 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG725/ADG731 requires an 8-bit data-word with data valid on the falling edge of SCLK.

Figures 4–7 illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

ADSP-21xx to ADG725/ADG731 Interface

The ADSP-21xx family of DSPs are easily interfaced to the ADG725/ADG731 without the need for extra logic. Figure 4 shows an example of an SPI interface between the ADG725/ADG731 and the ADSP-2191M. SCK of the ADSP-2191M drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case $\overline{\text{SPIxSEL}}$.

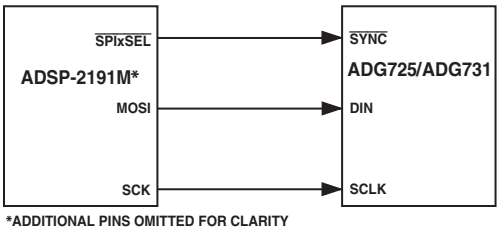


Figure 4. ADSP-2191M to ADG725/ADG731 Interface

A serial interface between the ADG725/ADG731 and the ADSP-2191M SPORT is shown in Figure 5. In this interface example, SPORT0 is used to transfer data to the switch. Transmission is initiated by writing a word to the Tx Register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the ADG725/ADG731 on the falling edge of its SCLK. The update of each switch condition takes place automatically after the eighth SCLK falling edge, regardless of the frame sync condition.

Communication between two devices at a given clock speed is possible when the following specs are compatible: frame sync delay and frame sync setup and hold, data delay and data setup and hold, and SCLK width. The ADG725/ADG31 expects a t_4 ($\overline{SYNC}$ falling edge to SCLK falling edge set-up time) of 13 ns minimum. Consult the ADSP-21xx User Manual for information on clock and frame sync frequencies for the SPORT Register.

The SPORT Control Register should be set up as follows:

TFSW = 1, Alternate Framing

INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

ISCLK = 1, Internal Serial Clock

TFSR = 1, Frame Every Word

ITFS = 1, Internal Framing Signal

SLEN = 0111, 8-Bit Data-Word

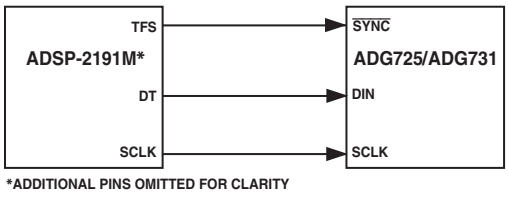


Figure 5. ADSP-2191M to ADG725/ADG731 Interface

8051 to ADG725/ADG731 Interface

A serial interface between the ADG725/ADG731 and the 8051 is shown in Figure 6. TXD of the 8051 drives SCLK of the ADG725/ADG731, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$.

The 8051 provides the LSB of its SBUF Register as the first bit in the data stream. The user will have to ensure that the data in the SBUF Register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result, no glue logic is required between the ADG725/ADG731 and microcontroller interface.

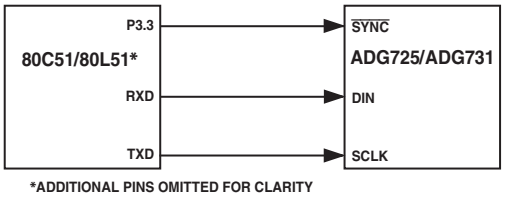


Figure 6. 8051 to ADG725/ADG731 Interface

MC68HC11 Interface to ADG725/ADG731

Figure 7 shows an example of a serial interface between the ADG725/ADG731 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{SYNC}$ is driven from one of the port lines, in this case PC7. The 68HC11 is configured for Master Mode: MSTR = 1, CPOL = 0, and CPHA = 1. When data is transferred to the part, PC7 is taken low, and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

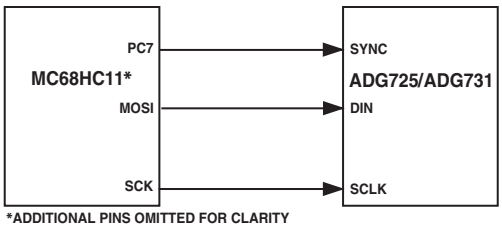


Figure 7. MC68HC11 Interface to ADG725/ADG731

APPLICATION CIRCUITS

ADG725/ADG731 in an Optical Network Control Loop

The ADG725/ADG731 can be used in optical network applications that have higher port counts and greater multiplexing requirements. The ADG725/ADG731 are well suited to these applications because they allow a single control circuit to connect a higher number of channels without increasing board size and design complexity.

In the circuit shown in Figure 8, the 0 V to 5 V outputs of the AD5532HS are amplified to a range of 0 V to 180 V and then used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor readings are muxed using the ADG731, a 32-channel switch, and fed back to a single-channel 14-bit ADC (AD7894).

The control loop is driven by an ADSP-2191L, a 32-bit DSP with an SPI compatible SPORT interface. It writes data to the DAC, controls the multiplexer, and reads data from the ADC via a 3-wire serial interface.

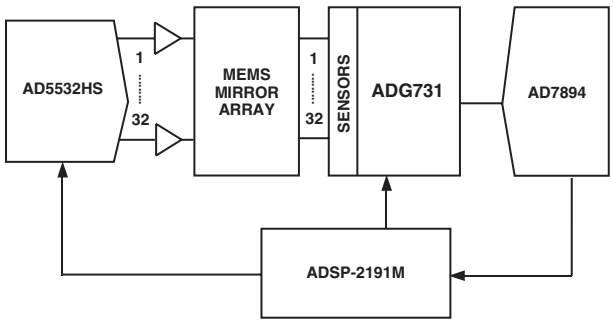


Figure 8. Optical Network Control Loop

Expand the Number of Selectable Serial Devices Using the ADG725/ADG731

The $\overline{SYNC}$ pin of the ADG725/ADG731 can be used to select one of a number of multiplexers. All devices receive the same serial clock and serial data, but only one device will receive the

$\overline{\text{SYNC}}$ signal at any one time. The mux addressed will be determined by the decoder. There will be some digital feedthrough from the digital input lines. Using a burst clock will minimize the effects of digital feedthrough on the analog signal channels. Figure 9 shows a typical circuit.

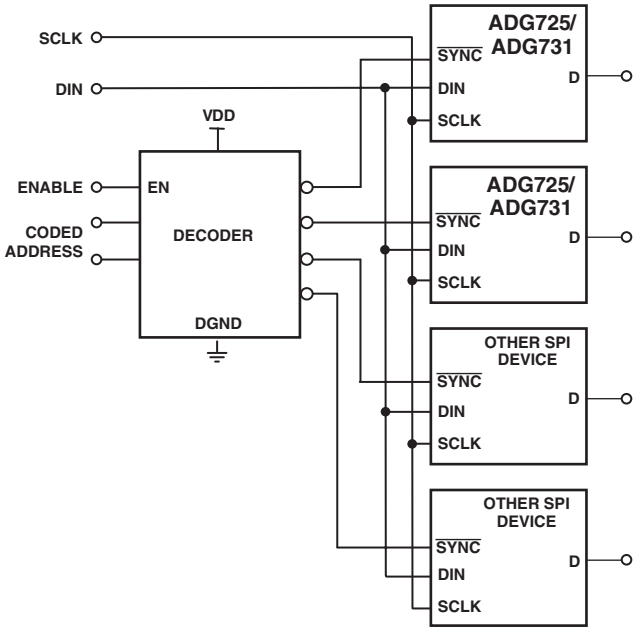
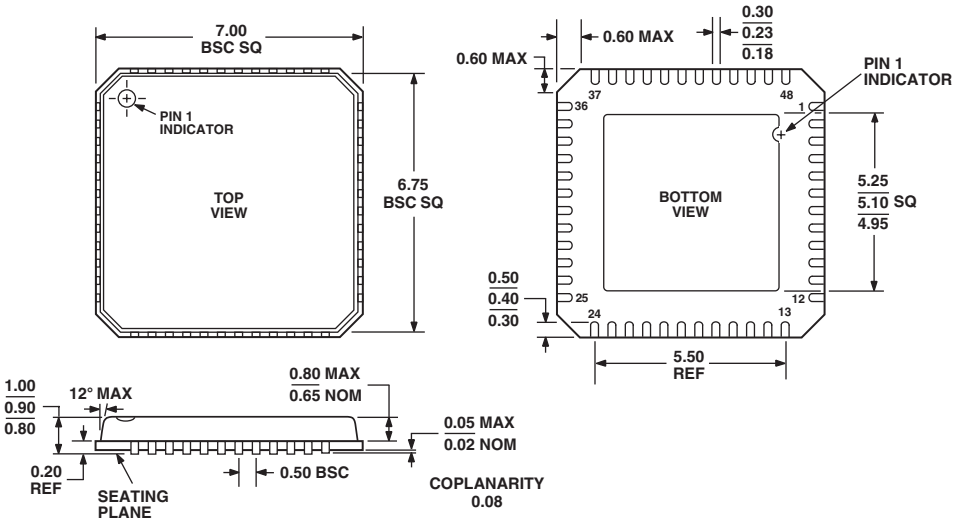


Figure 9. Addressing Multiple ADG725/ADG731s Using a Decoder

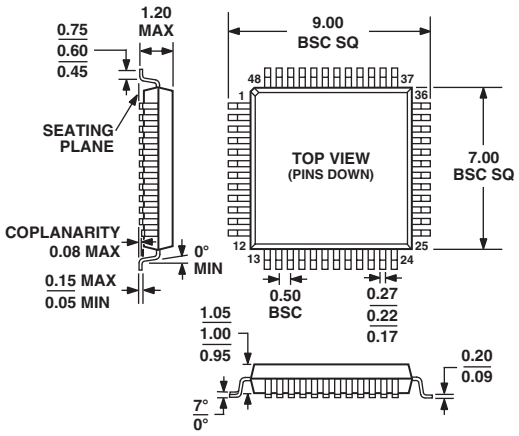
OUTLINE DIMENSIONS

48-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

48-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026ABC

Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
Edits to ORDERING GUIDE	6
Edits to PIN CONFIGURATIONS	7
Edits to PIN FUNCTION DESCRIPTIONS	7
Changes to Test Circuit 3	11
Updated OUTLINE DIMENSIONS	16